PRAYAS

JEE 2025

Lecture - 01

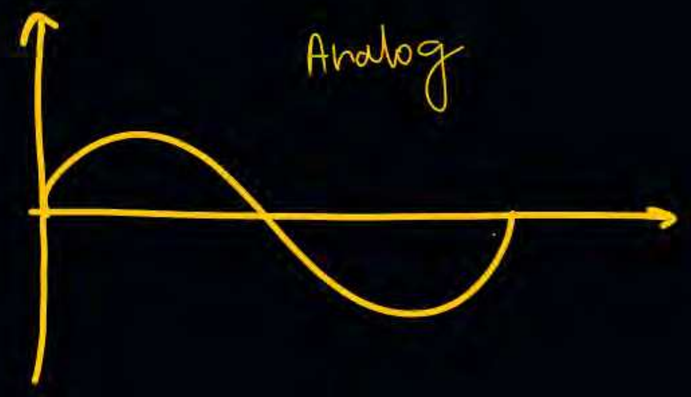
Physics

Semiconductor

By- Saleem Ahmed Sir

Topics *to be covered*

1. Logic Gates
2.
3.
4.



ATDB.uno

1 ⟶ ON switch, High sigh , +5V

0 ⟶ OFF switch, Low Signal , +0V

ATDB.uno

Boolen Algebra

+, −, x, ÷, %

ATDB.uno

Boolen Algebra

OR

$A + B = Y$

- $0 + 0 = 0$
- $0 + 1 = 1$
- $1 + 0 = 1$
- $1 + 1 = 1$

AND $\equiv A.B = Y$

- $0 . 1 = 0$
- $1 . 0 = 0$
- $0 . 0 = 0$
- $1 . 1 = 1$

- $A + 1 = 1$
- $A + 0 = A$
- $A . 0 = 0$
- $A . 1 = A$

- $\overline{1} = 0$
- $\overline{0} = 1$
- $Y = A \Rightarrow \overline{Y} = \overline{A}$

$A.(B+C) = A.B + A.C$

$(A+B).(C+D) = A.C + A.D + B.C + B.D$

- $A + B = B + A$
- $(A+B) + C = A + (B+C)$
- $A + \overline{A} = 1$
- $A . \overline{A} = 0$
- $A + A = A$
- $A . A = A$

(Demorgan theorm)

$$\overline{A+B} = \overline{A} \cdot \overline{B}$$

$$\overline{A \cdot B} = \overline{A} + \overline{B}$$

Q simplify the following booken expression

① $A \cdot (A+B) = A \cdot A + A \cdot B = A + A \cdot B = A(1+B)$
$= A \cdot 1 = A$

② $A \cdot (\overline{A} + B) = A \cdot \overline{A} + A \cdot B = 0 + A \cdot B = AB$

③ $(A+B)(\overline{A}+\overline{B}) = A \cdot \overline{A} + A \cdot \overline{B} + B \cdot \overline{A} + B \cdot \overline{B}$
$= A \cdot \overline{B} + B \cdot \overline{A}$

④ $(A+\overline{B}) \cdot (\overline{A}+B) = AB + \overline{B} \cdot \overline{A}$

(5) $\overline{\overline{A}} = A$

(6) $\overline{A + B} = \overline{x + y} = \overline{x} \cdot \overline{y} = \overline{\overline{A}} \cdot \overline{\overline{B}} = A \cdot B$

(7) $\overline{A \cdot B} = \overline{x \cdot y} = \overline{x} + \overline{y} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$

(8) $(A+B)\cdot(A+C) = A + AC + BA + B \cdot C$

$= A(1 + C + B) + B \cdot C$

$= A \cdot 1 + B \cdot C$

$= A + BC$

(9) $Y = A\overline{B} + \overline{A}B \Rightarrow$ XOR

find $\overline{Y}$

$\overline{Y} = \overline{A\overline{B} + \overline{A}B} = \overline{x + y} = \overline{x} \cdot \overline{y}$

$\overline{Y} = \overline{A\overline{B}} \cdot \overline{\overline{A}B} = (\overline{A} + \overline{\overline{B}}) \cdot (\overline{\overline{A}} + \overline{B})$

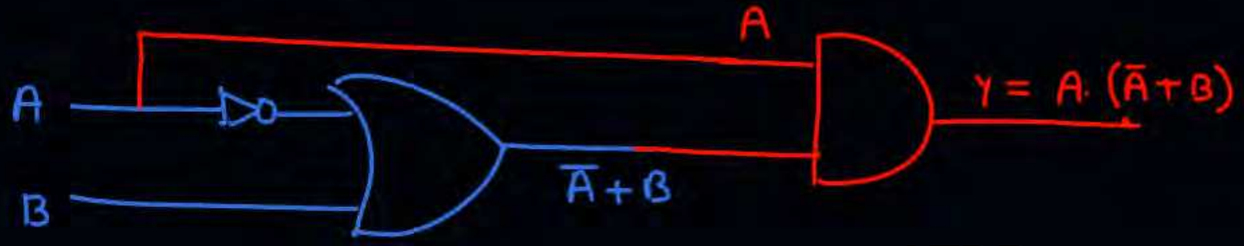
$= (\overline{A} + B) \cdot (A + \overline{B})$

$= 0 + \overline{A} \cdot \overline{B} + B \cdot A + 0$

$= AB + \overline{A} \cdot \overline{B} \equiv$ XNOR

Q1 $A.(A+B) = A + AB = A(1+B) = A \cdot 1 = A$

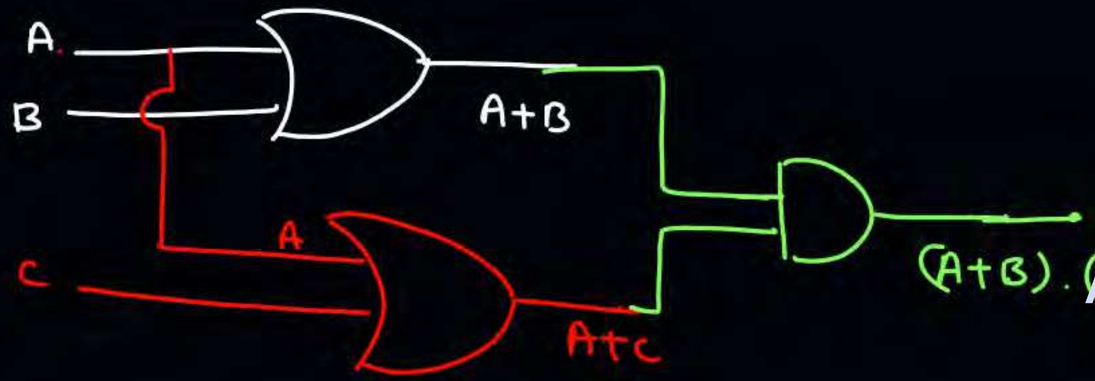
Q2 $A.(\overline{A}+B) = A \cdot \overline{A} + A \cdot B = 0 + A \cdot B = AB$

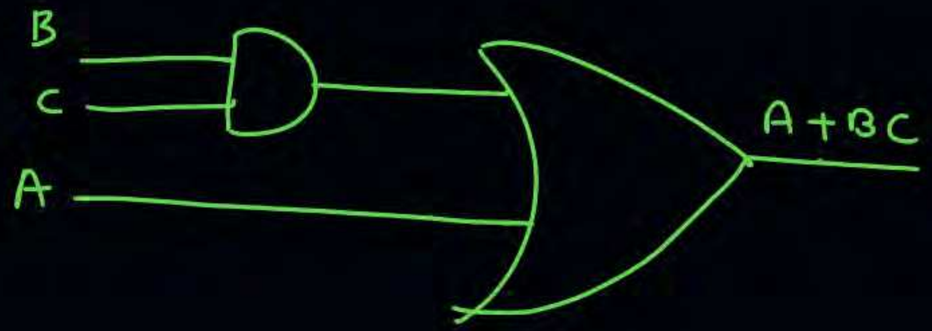


ATDB.uno

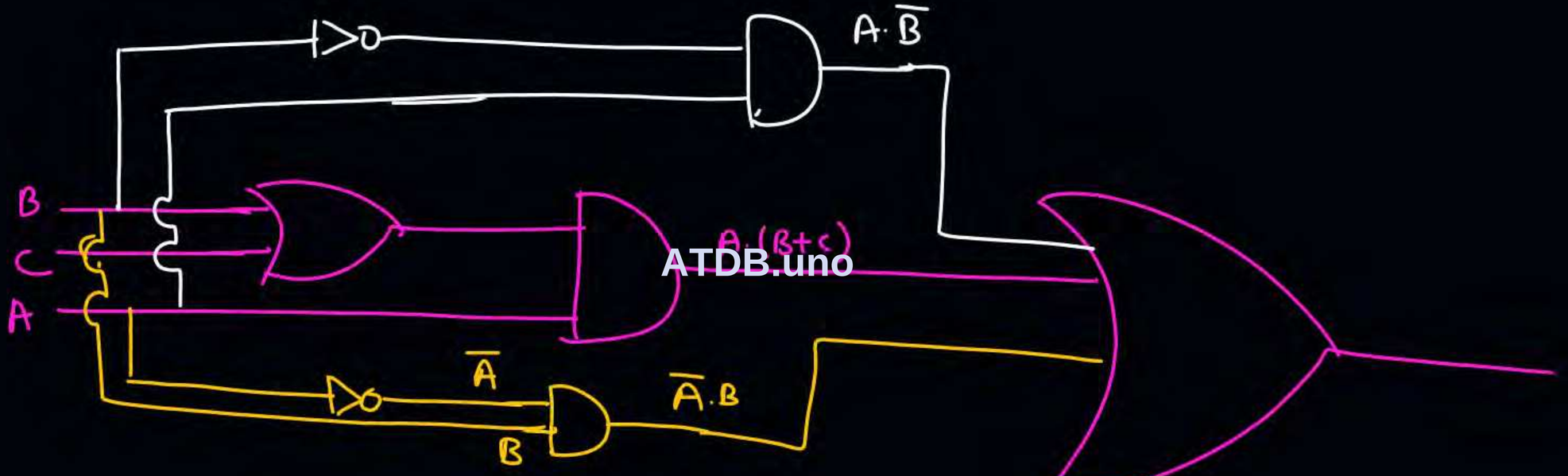
Q $(A+B).(A+C) =$ ⟶ $A + AC + AB + BC$

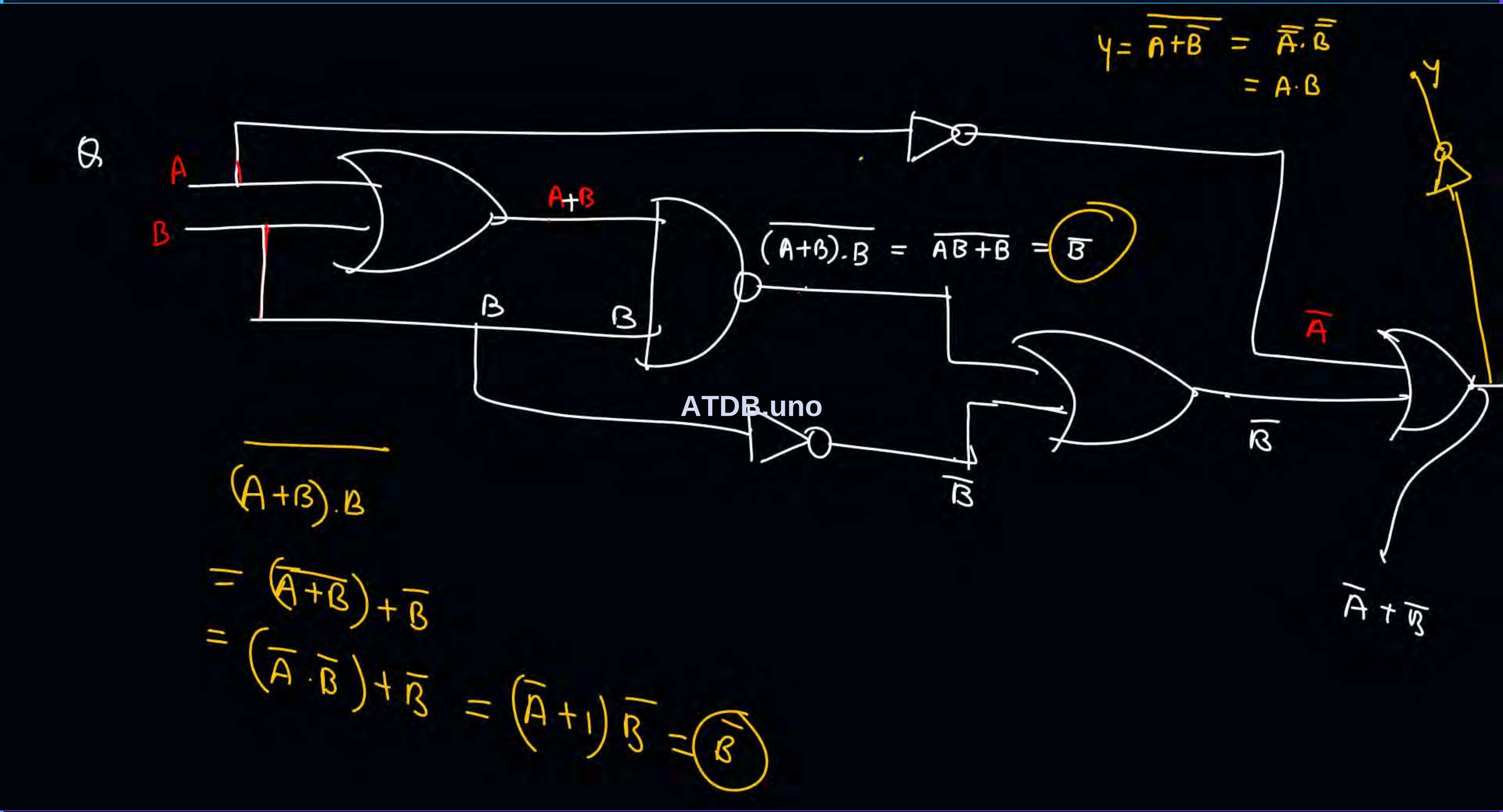
$= A(1+C+B) + BC = A + BC$





$$A \cdot (B+C) + (\overline{A} \cdot B) \oplus (A \cdot \overline{B})$$

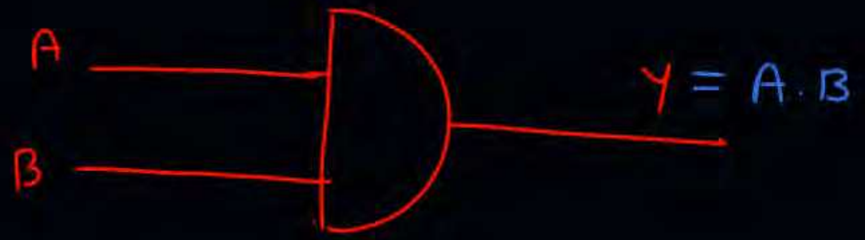




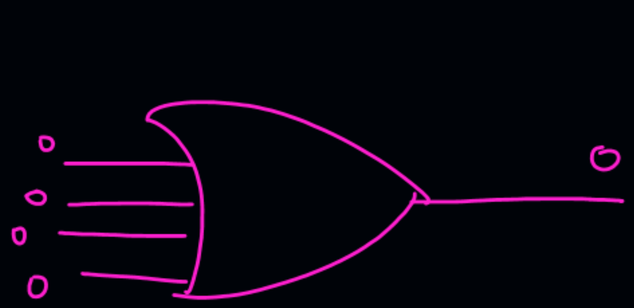
OR Gate

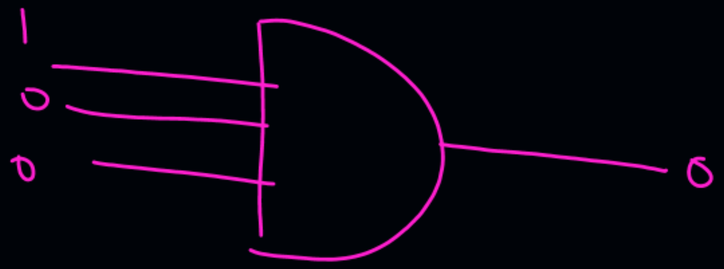
A	B	Y = A + B
0	0	0
0	1	1
1	0	1
1	1	1

AND Gate

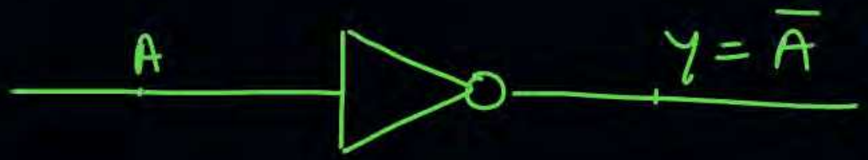


A	B	Y = A · B
0	0	0
0	1	0
1	0	0
1	1	1



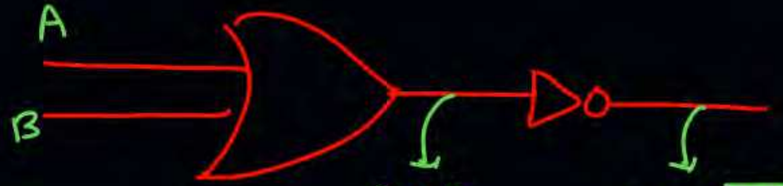


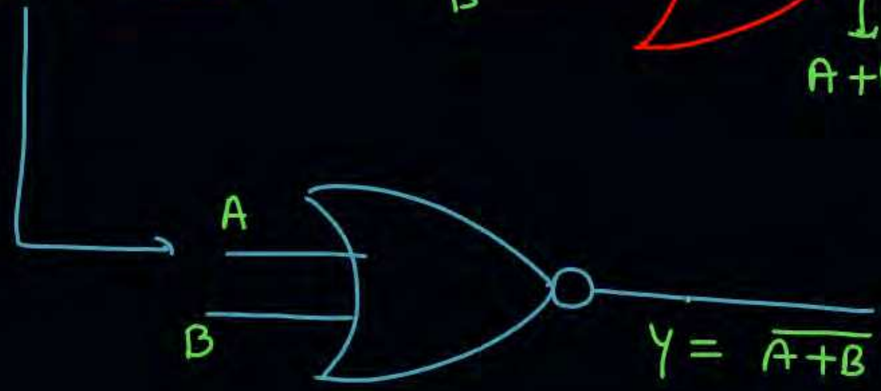
NOT Gate (Reverse) / Invert



A	Y = Ā
0	1
1	0

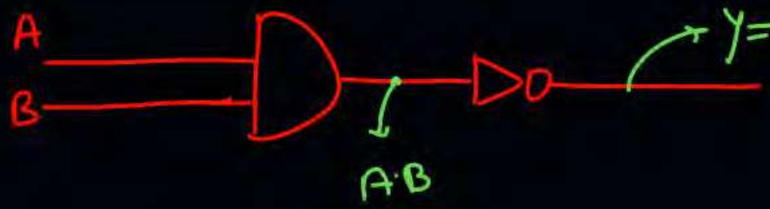
NOR Gate



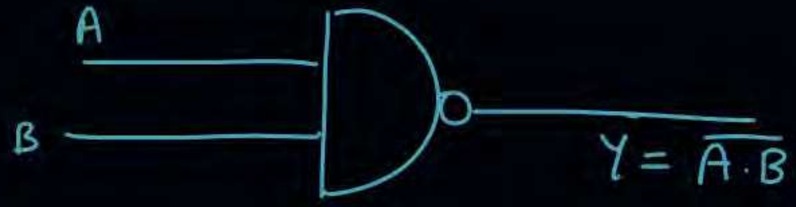


A	B	OR A + B	NOR Y = A+B
0	0	0	1
0	1	1	0
1	0	1	0
1	1	1	0

NAND Gate



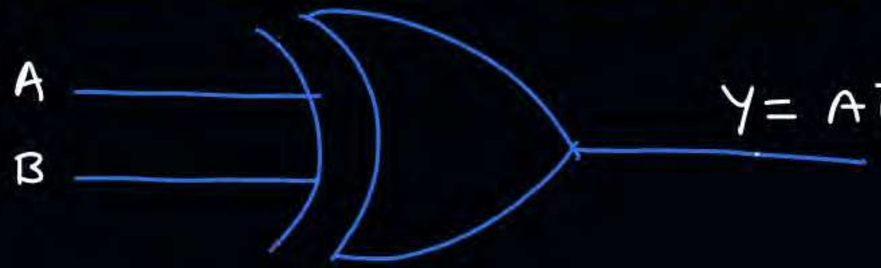
$$Y = \overline{A \cdot B} = \bar{A} + \bar{B}$$



$$Y = \overline{A \cdot B}$$

A	B	A·B	$\overline{A \cdot B} = Y$
0	0	0	1
0	1	0	1
1	0	0	1
1	1	1	0

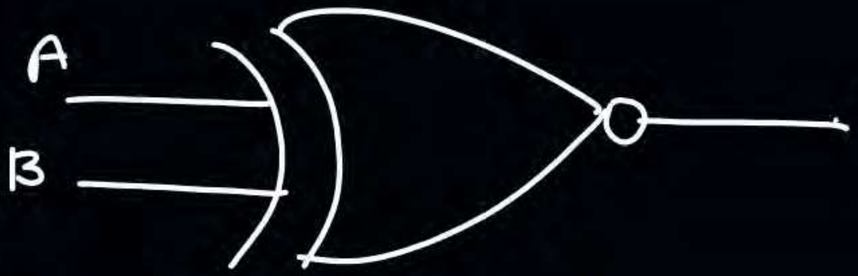
XOR Gate // EXOR gate



$$Y = A\bar{B} + \bar{A}B$$

A	B	$A\bar{B}$	$\bar{A}B$	$\bar{A}B + A\bar{B} = Y$
0	0	0	0	0
0	1	0	1	1
1	0	1	0	1
1	1	0	0	0

EXNOR Gate / XNOR



$$Y = \overline{A\bar{B} + \bar{A}B} = AB + \bar{A}.\bar{B}$$

A	B	$Y = AB + \bar{A}.\bar{B}$
0	0	1
0	1	0
1	0	0
1	1	1

$$Y = \overline{A\bar{B} + \bar{A}B} \equiv \overline{EXOR} = EXNOR$$

$$= \overline{A\bar{B}} \cdot \overline{\bar{A}B}$$

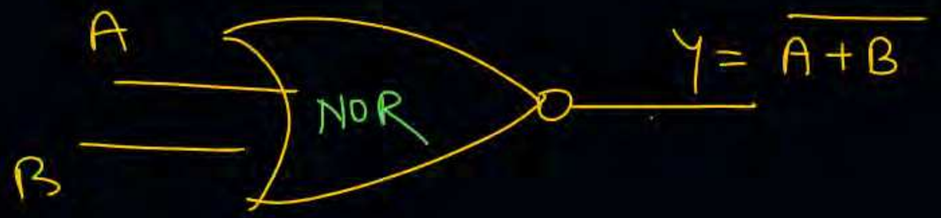
$$= (\bar{A} + \bar{\bar{B}}) \cdot (\bar{\bar{A}} + \bar{B})$$

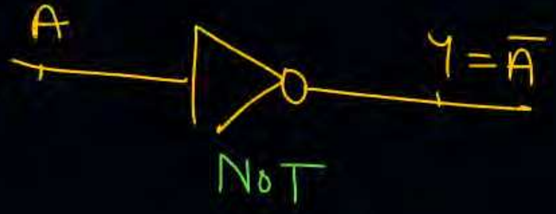
$$= (\bar{A} + B) \cdot (A + \bar{B})$$

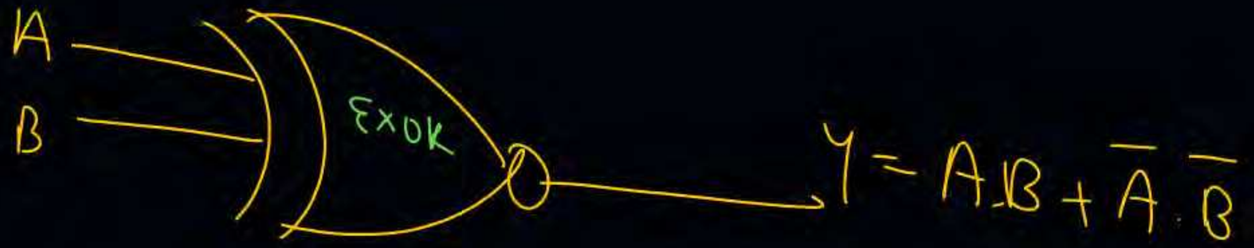
$$= 0 + \bar{A} \cdot \bar{B} + BA + 0$$

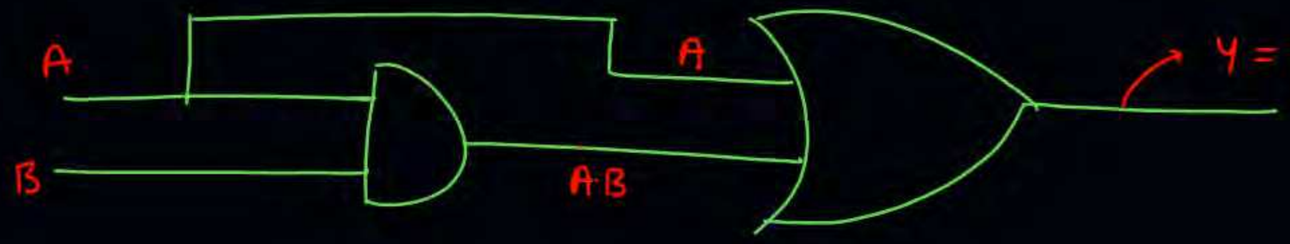
$$= AB + \bar{A} \cdot \bar{B}$$

ATDB.uno

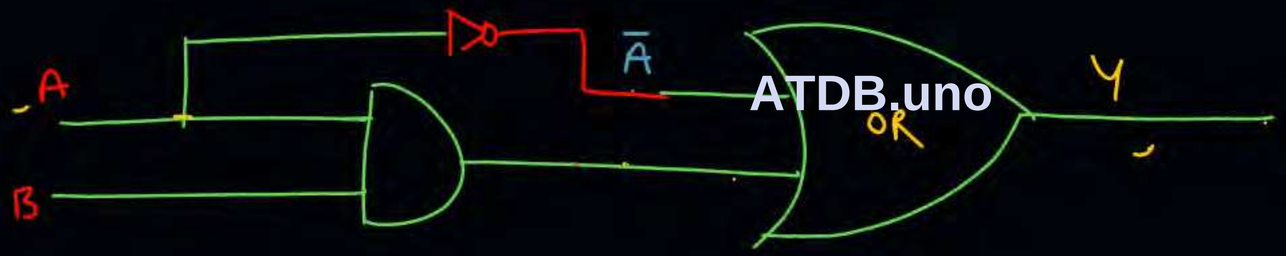






① 

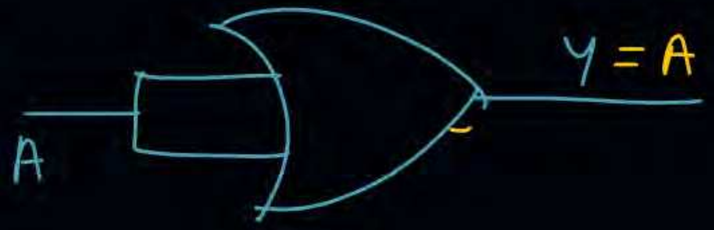
$Y = A + A \cdot B = A(1 + B) = A \cdot 1 = A$

② 

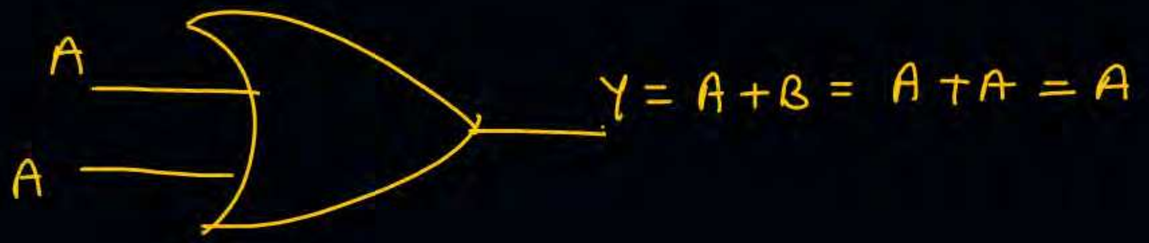
$Y = \bar{A} + AB$

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	1

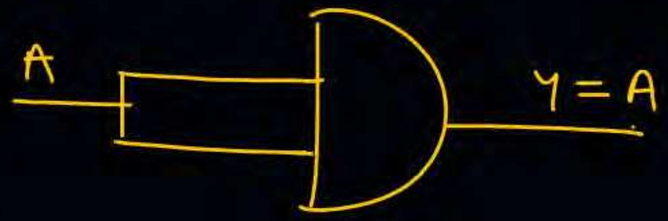
(3)



≡

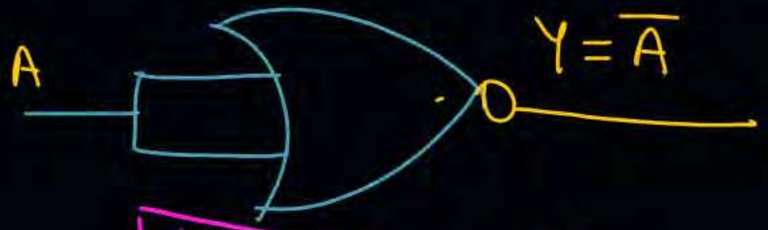


(4)



ATDB.uno

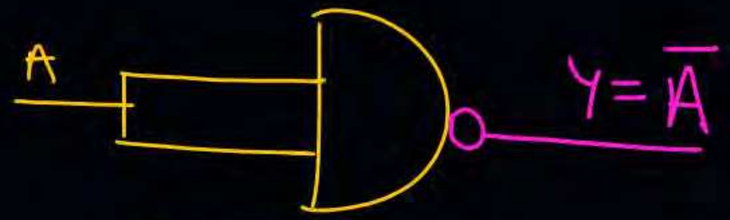
(*5)



like NOT

NOR

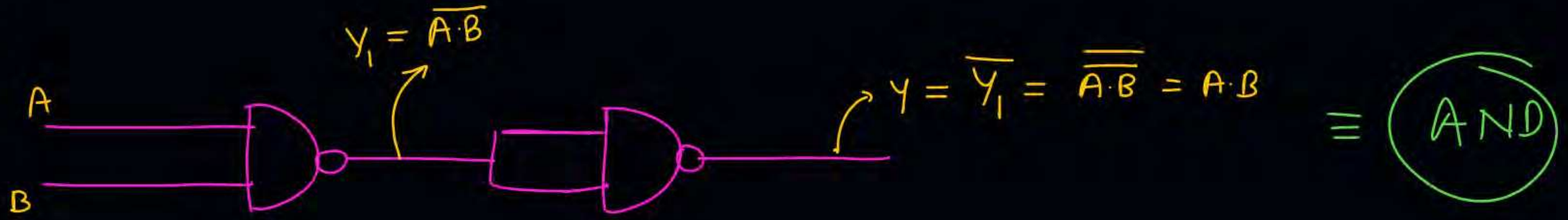
(6)



like NOT

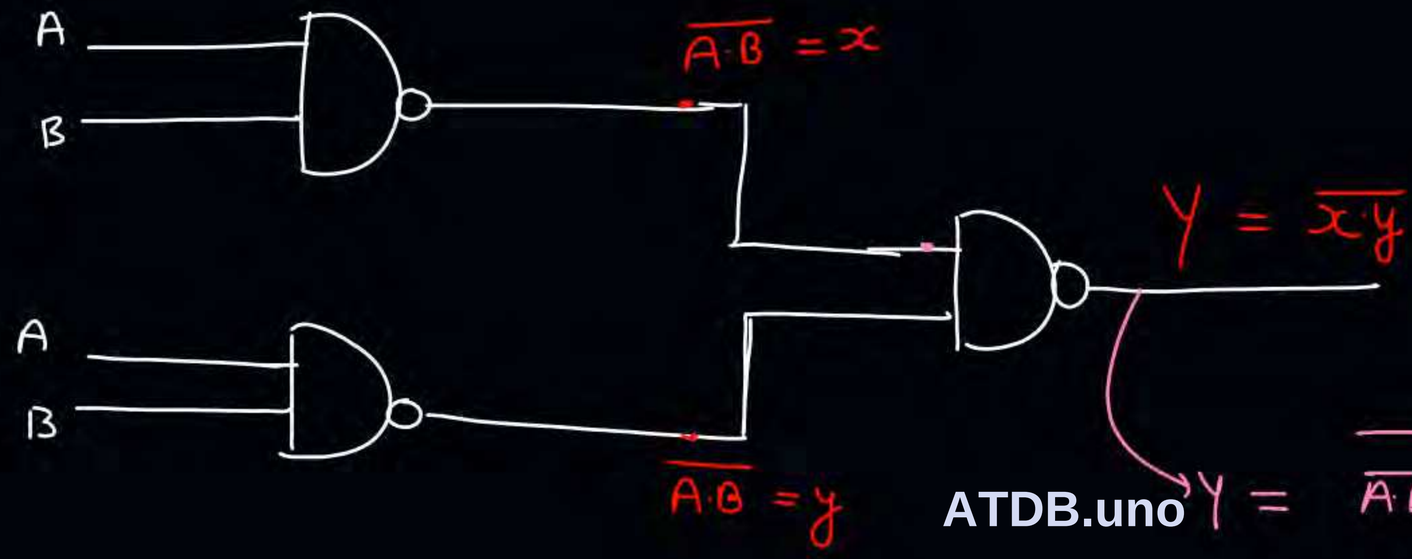
NAND

(7)



(8)

(g)

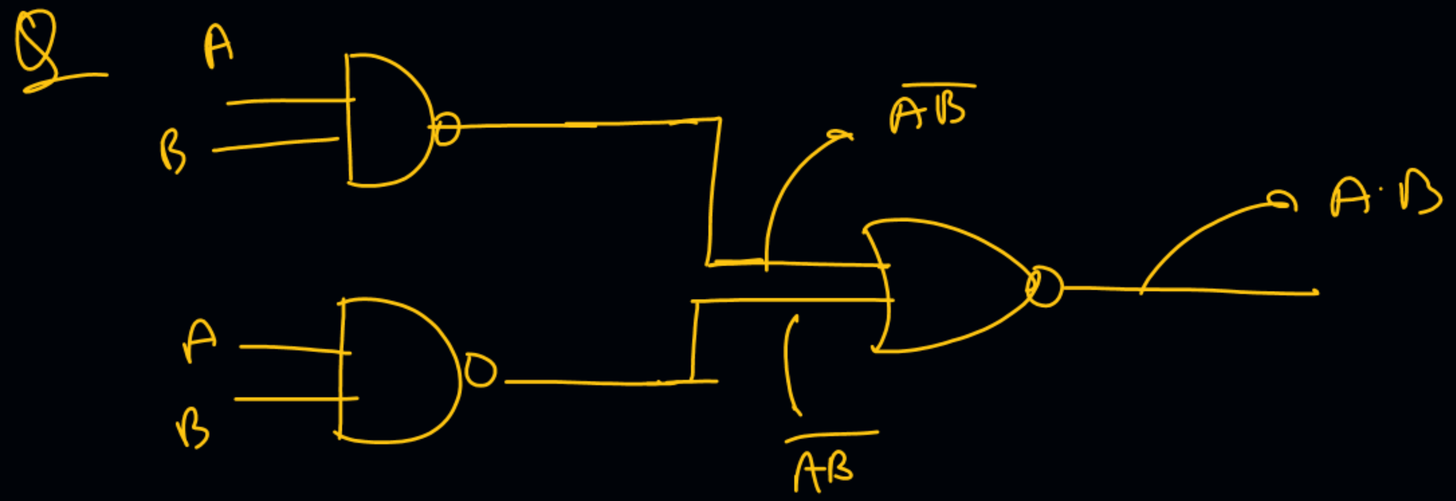


$$Y = \overline{x} + \overline{y}$$

$$= \overline{\overline{A \cdot B}} + \overline{\overline{A \cdot B}} = A \cdot B$$

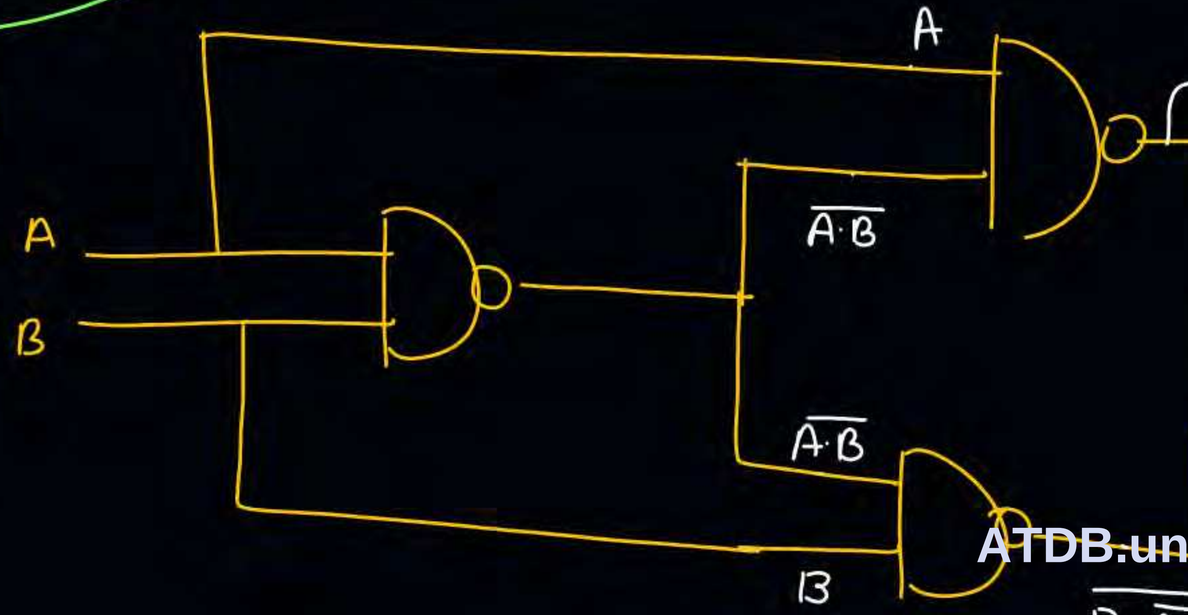
$$Y = \overline{\overline{A \cdot B} \cdot \overline{A \cdot B}}$$

$$= \overline{\overline{A \cdot B}} = A \cdot B$$



4-5 lines P40

Q



$\overline{A \cdot \overline{AB}} = \overline{A} + \overline{\overline{AB}} = \overline{A} + AB$

EXOR

$Y = \overline{(\overline{A} + AB) \cdot (\overline{B} + AB)}$

$= \overline{(\overline{A} + AB)} + \overline{(\overline{B} + AB)}$

$= \overline{\overline{A}} \cdot \overline{AB} + \overline{\overline{B}} \cdot \overline{AB}$

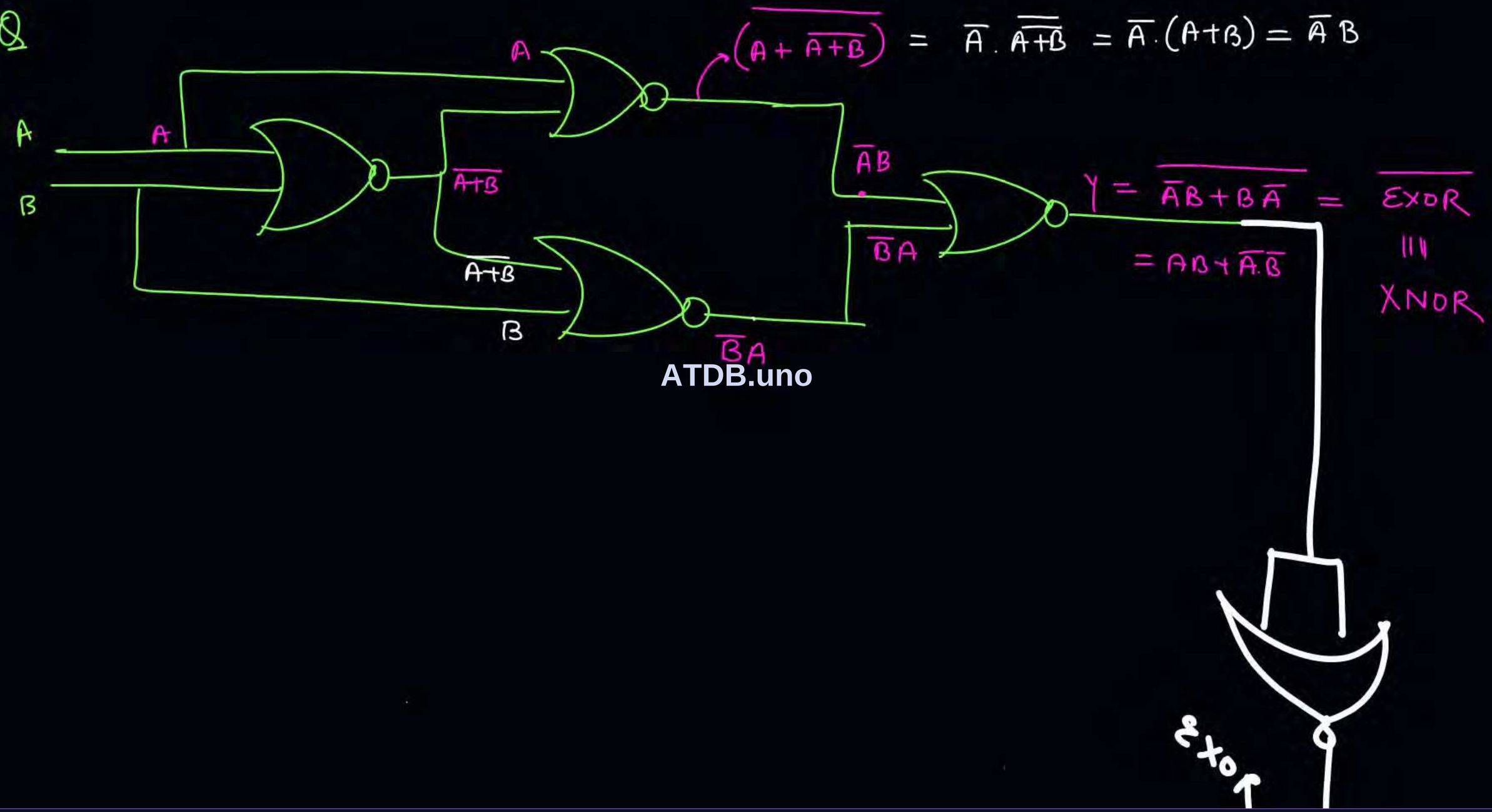
$= A \cdot (\overline{A} + \overline{B}) + B \cdot (\overline{A} + \overline{B})$

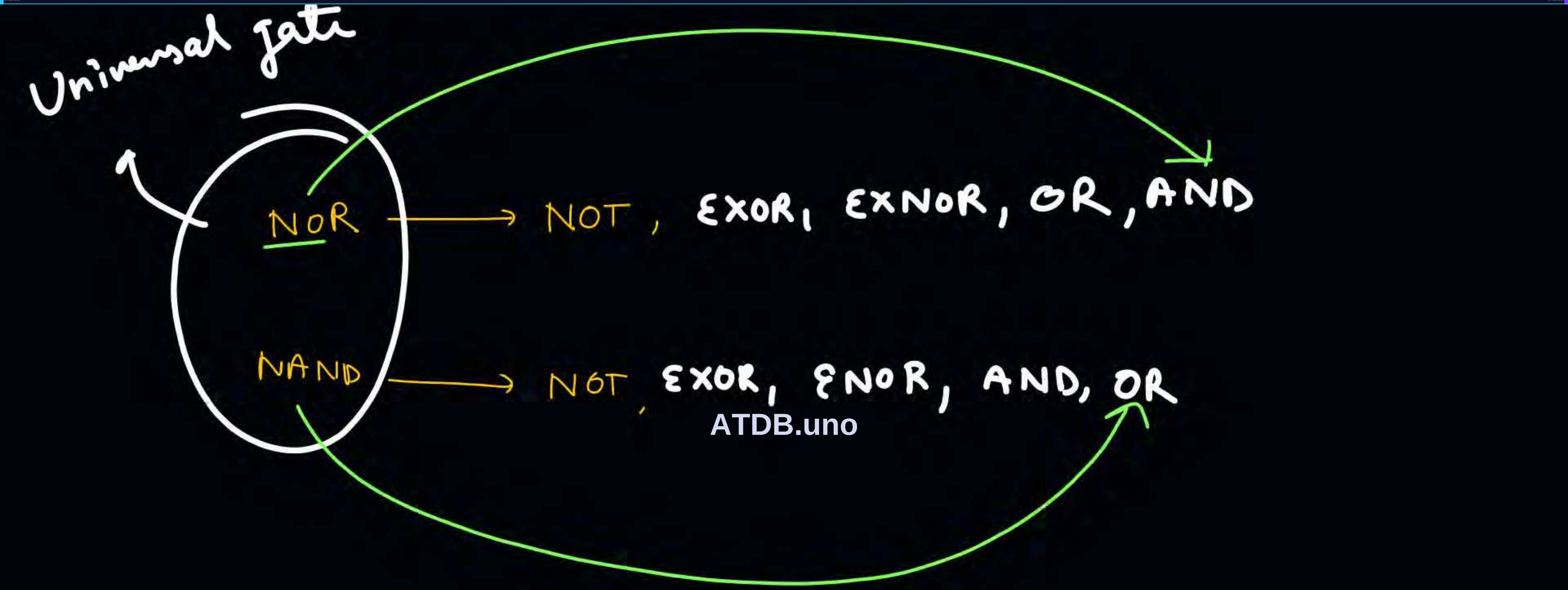
$= 0 + A\overline{B} + B\overline{A} + 0$

$= A\overline{B} + B\overline{A} \equiv$ EXOR

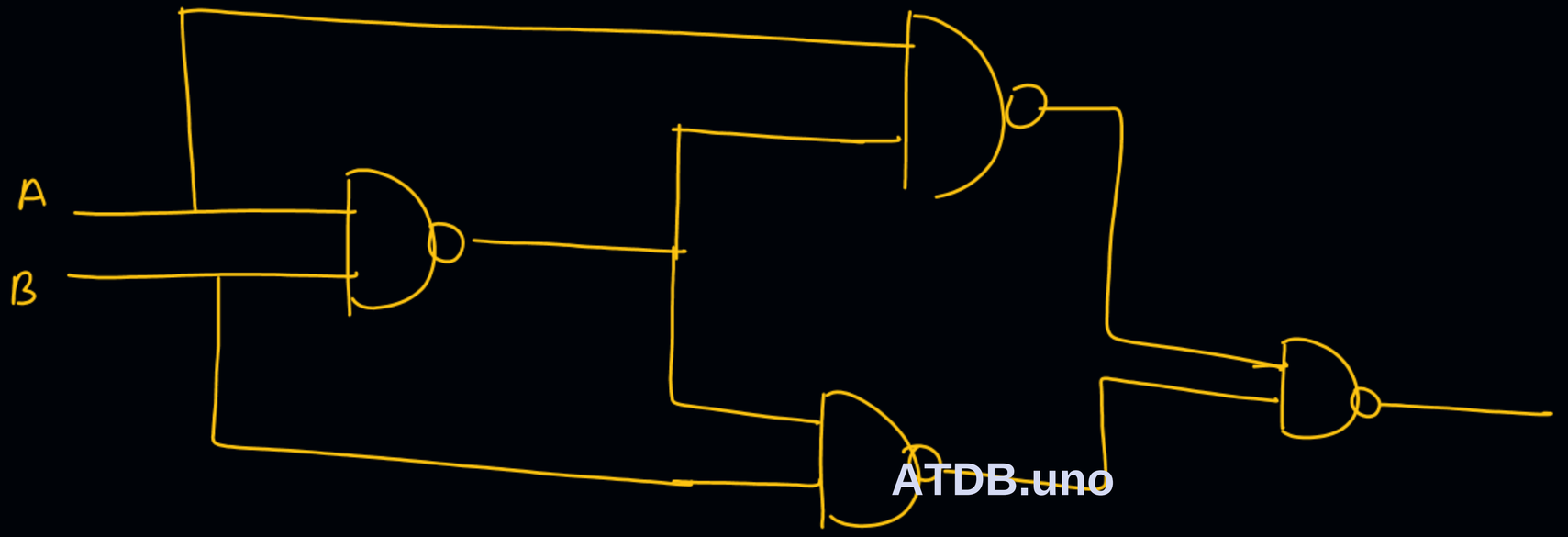
$= \overline{B} + AB$

Q1

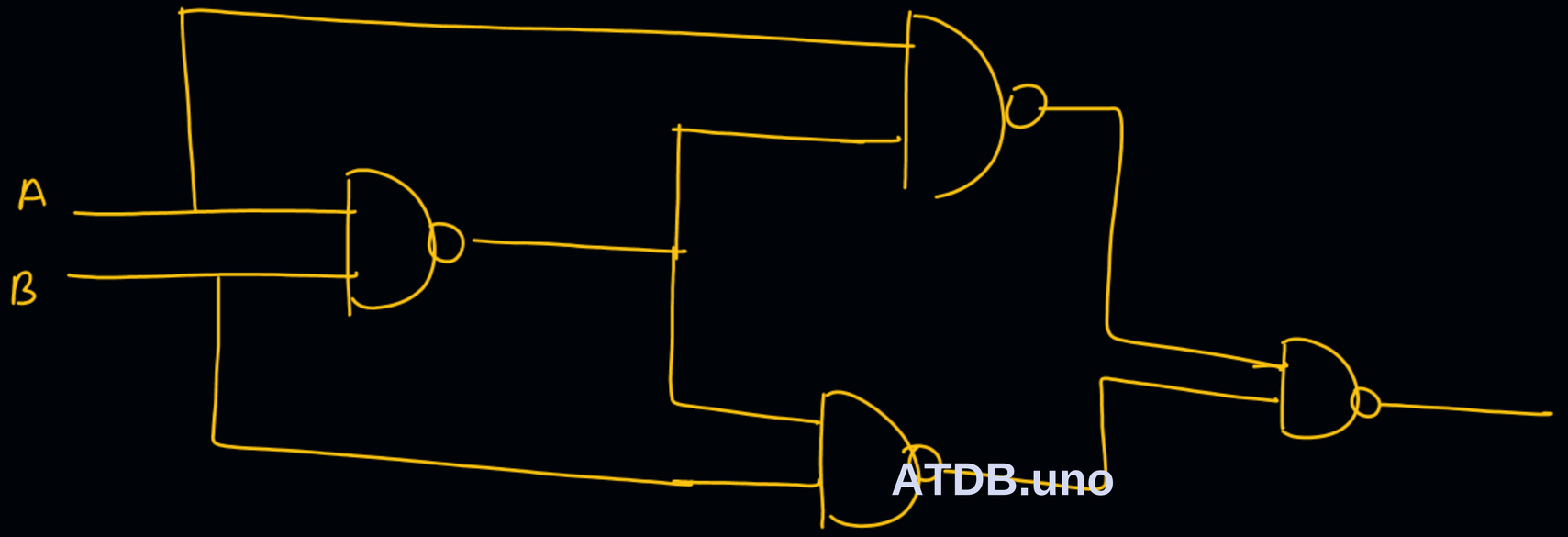


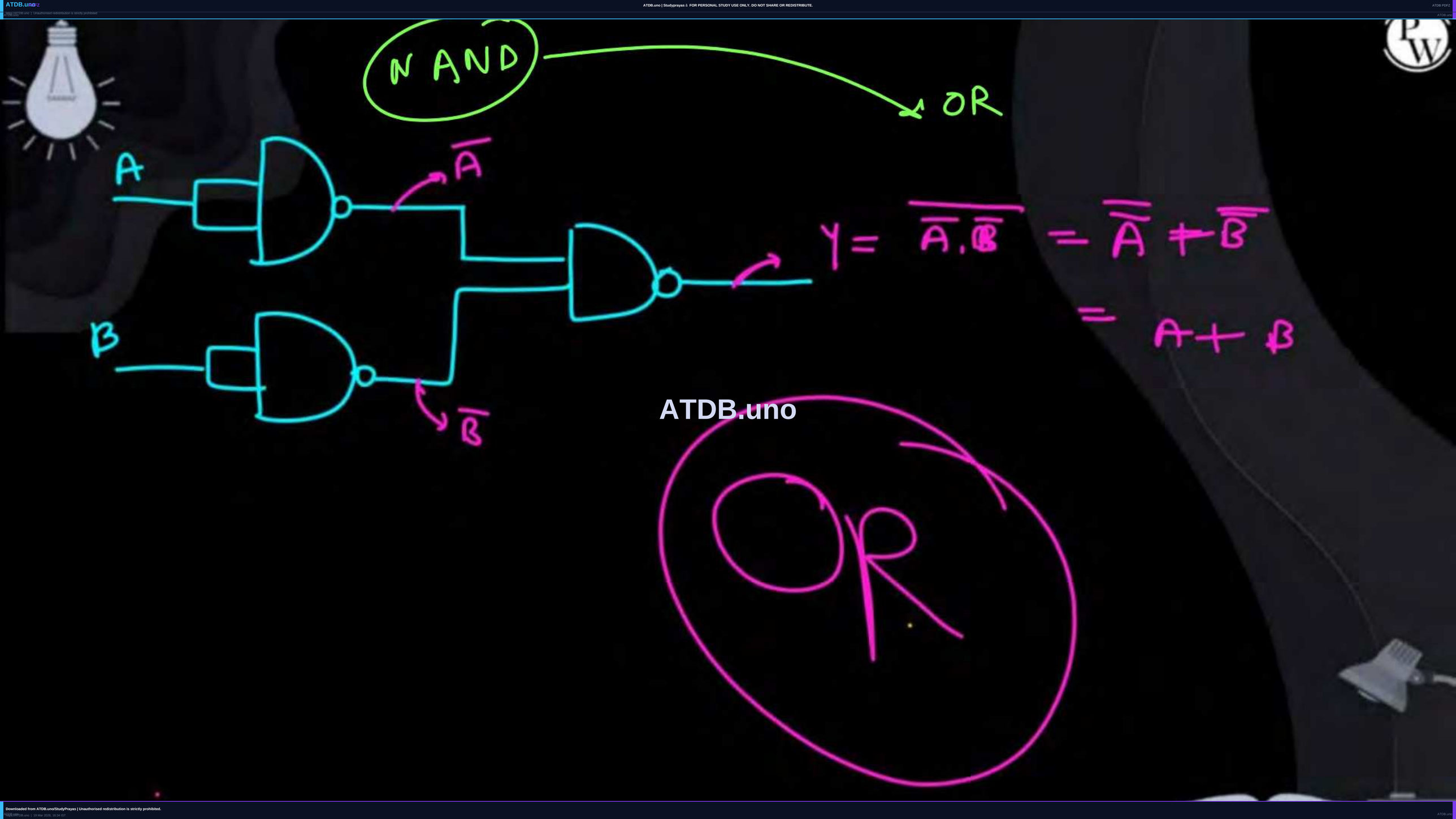


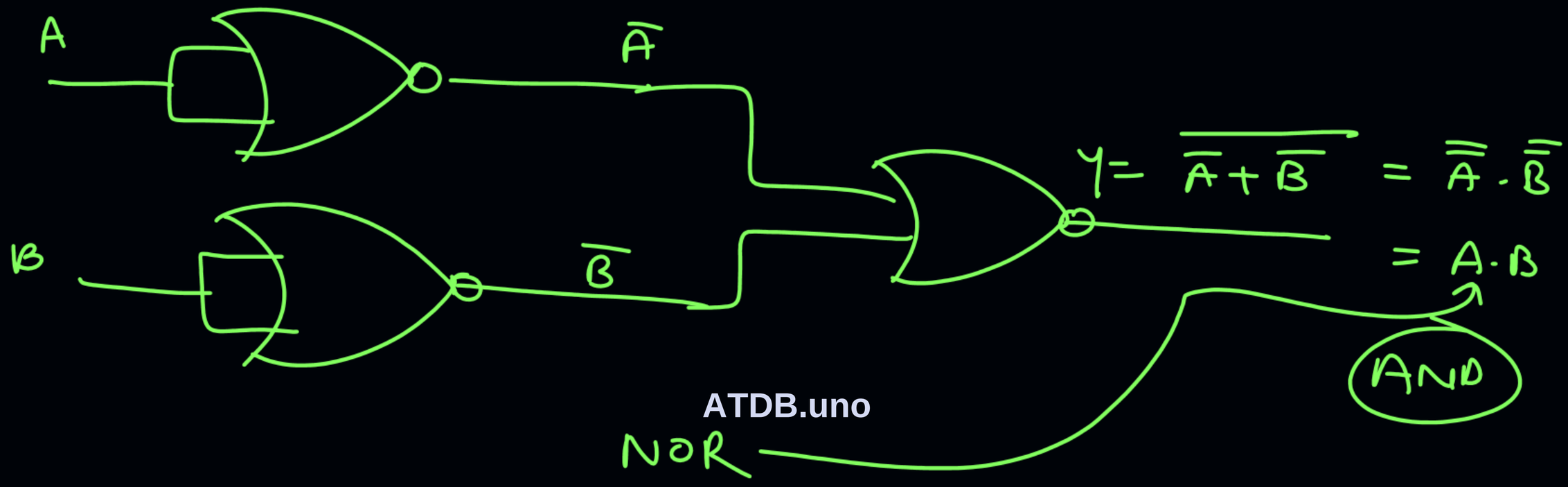
Q2

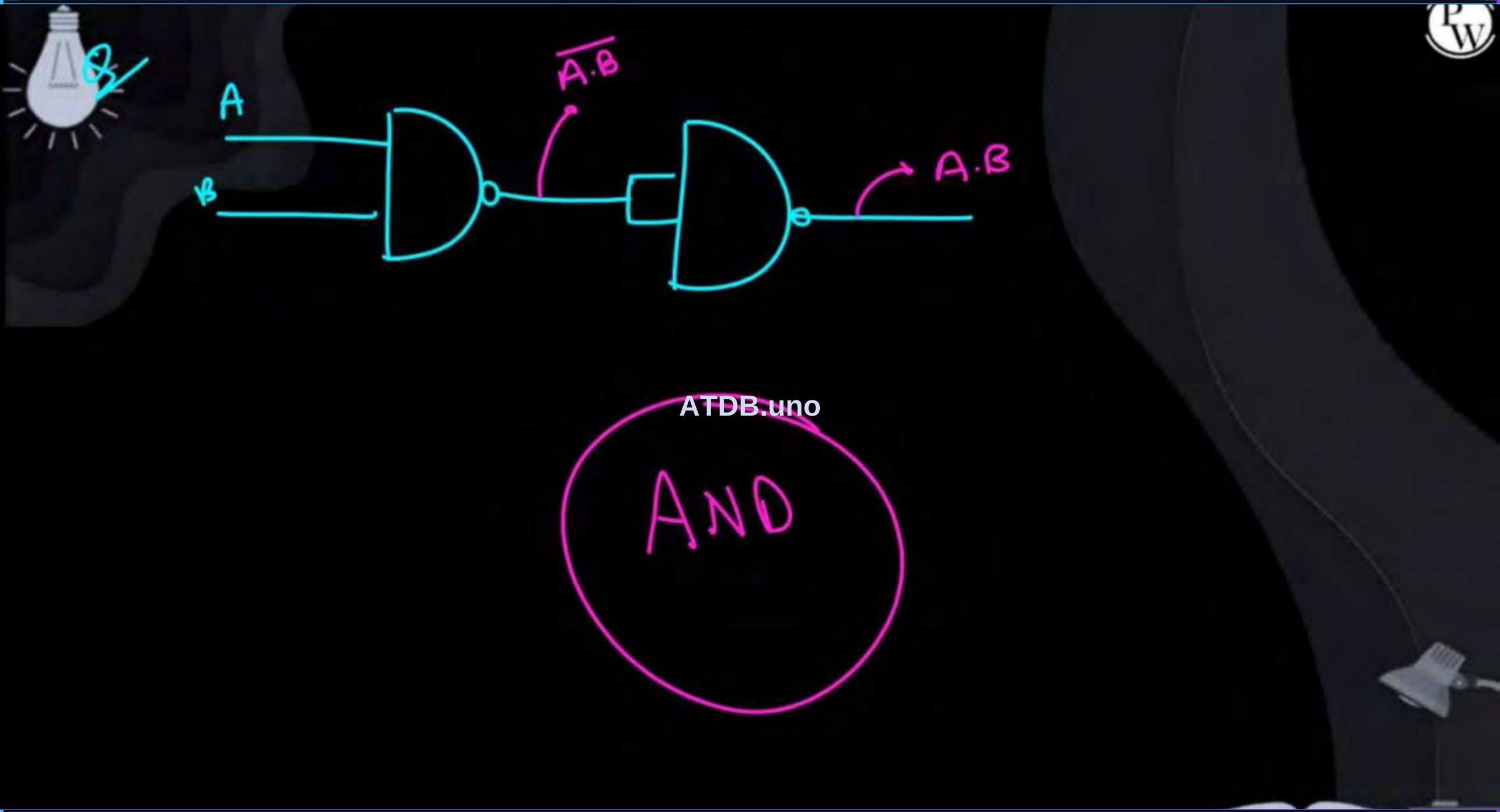


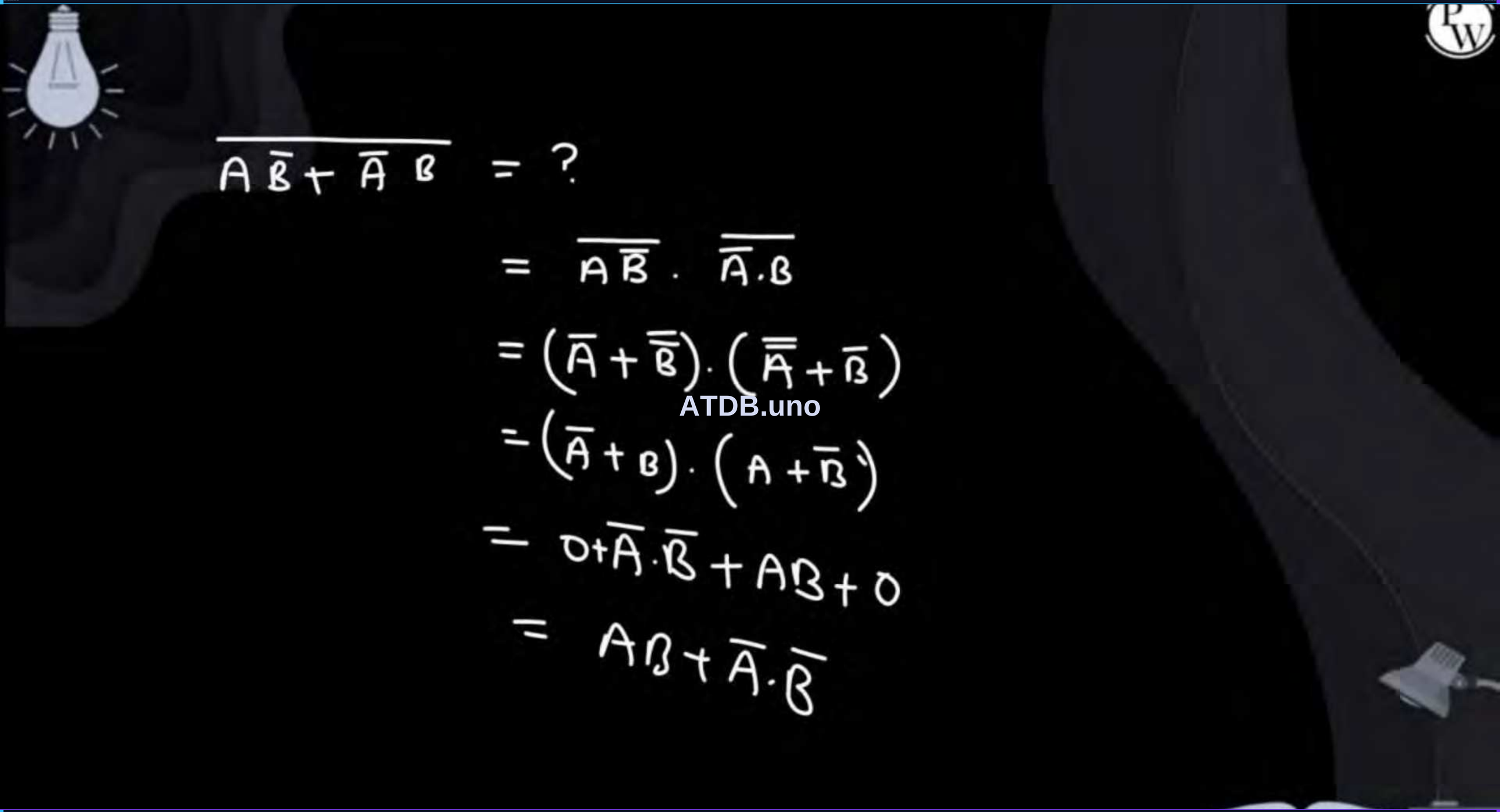
Q2



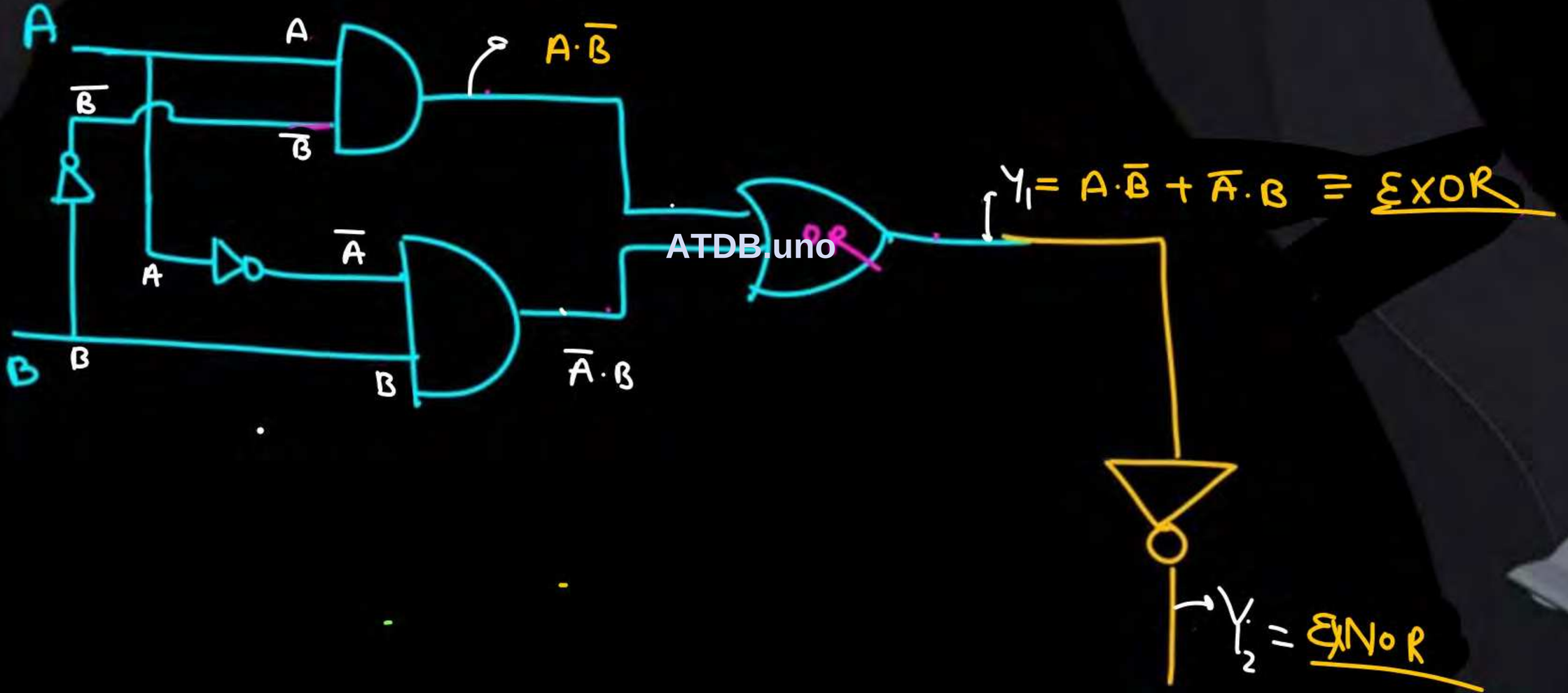








Q write actual logical expression



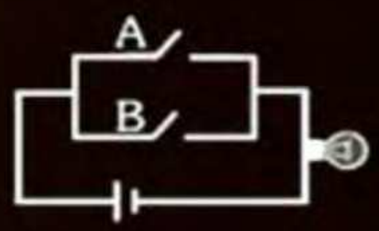
Summary of logic gates

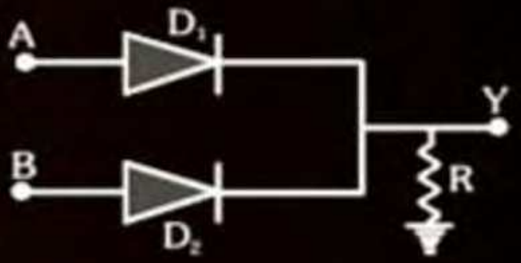
Names	Symbol	Boolean Expression	Truth table	Electrical analogue	Circuit diagram (Practical Realisation)

OR

$Y = A + B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

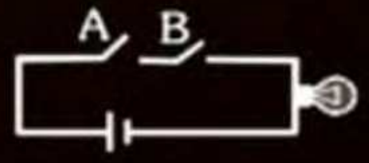


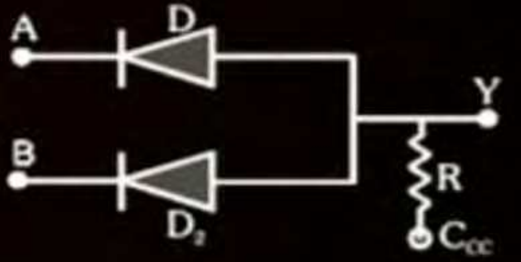


AND

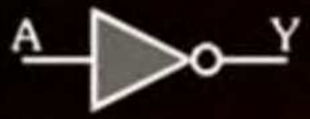
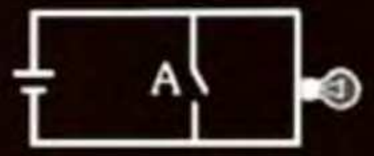
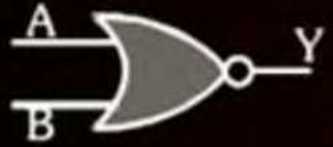
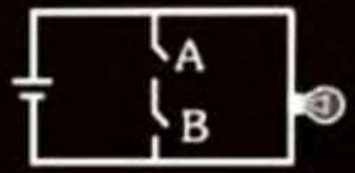
$Y = A.\ B$

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1





Summary of logic gates

Names	Symbol	Boolean Expression	Truth table	Electrical analogue	Circuit diagram (Practical Realisation)
NOT Inverter		$Y = \bar{A}$			
NOR (OR + NOT)		$Y = \overline{A+B}$			
NAND (AND + NOT)		$Y = \overline{A.B}$			

Summary of logic gates

Names	Symbol	Boolean Expression	Truth table	Electrical analogue	Circuit diagram (Practical Realisation)

XOR (Exclusive OR)

$$Y = A \oplus B$$

or

$$Y = \bar{A}.B + A\bar{B}$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

XNOR (Exclusive NOR)

$$Y = A \odot B$$

or

$$Y = A.B + \bar{A}.\bar{B}$$

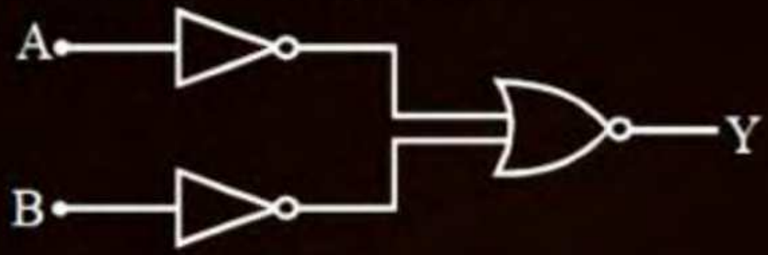
or

$$Y = \overline{A \oplus B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

QUESTION

The logic circuit shown below has the input wave forms 'A' and 'B' as shown. Pick out the correct output waveform. Output is: **[AIEEE-2009]**



1

2

3

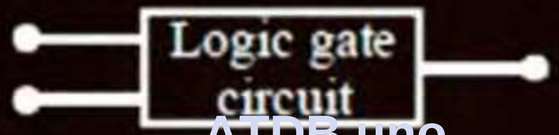
4

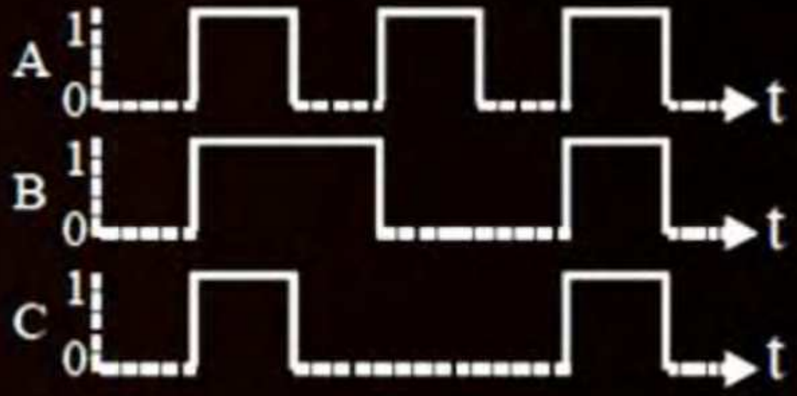
Ans. (1)

QUESTION

The following figure shows a logic gate circuit with two input A and B output C. The voltage waveforms of A, B and C are as shown in second figure below. The logic gate is:

1. OR gate
2. NAND gate
3. AND gate
4. NOR gate

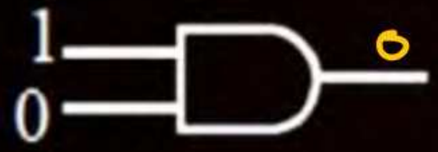




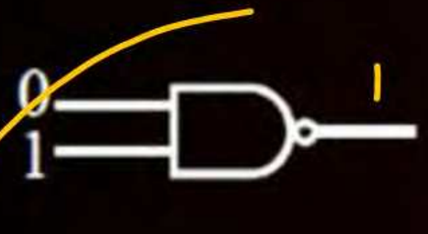
Ans. (3)

QUESTION

Which of the following gates will have an output of 1:

1. 

2. 

3. 

4. 

Ans. (3)

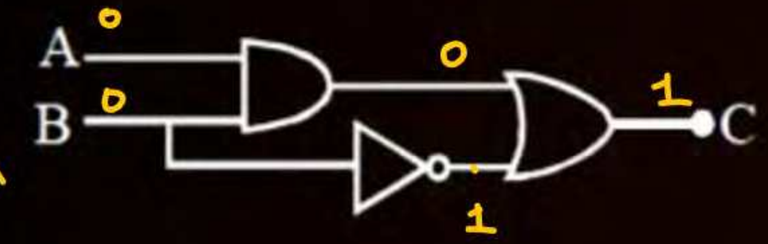
QUESTION

Which of the following circuits correctly represents the following truth table?

[JEE-Main Online-2013]

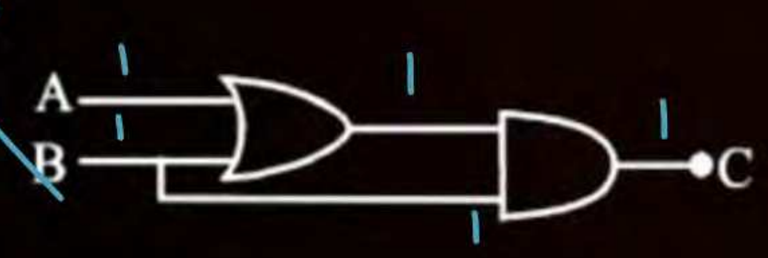
A	B	C
0	0	0
0	1	0
1	0	1
1	1	0

1

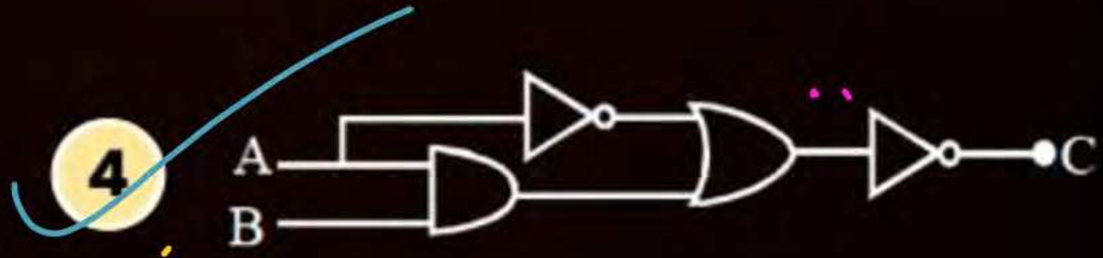


2

3



4



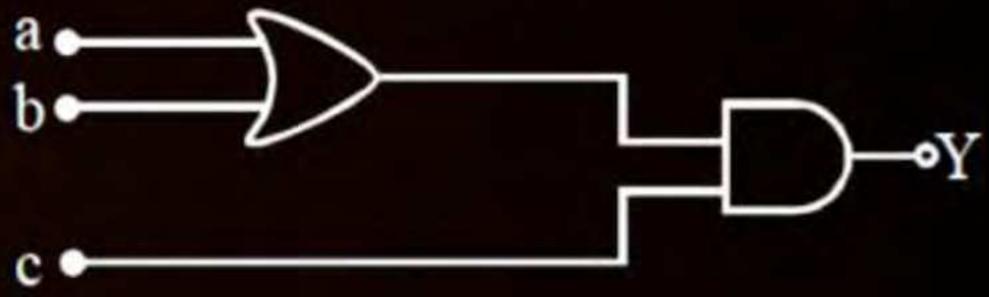
Ans. (4)

QUESTION

To get an output of 1 from the circuit shown in figure the input must be :-

[JEE-Main Online-2016]

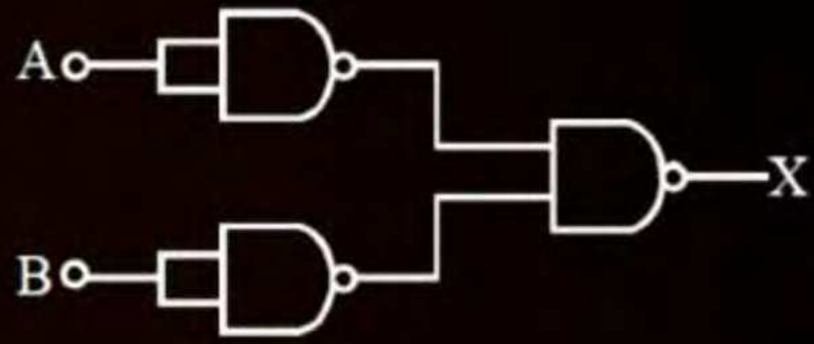
1. a = 1, b = 0, c = 1
2. a = 1, b = 0, c = 0
3. a = 0, b = 1, c = 0
4. a = 0, b = 0, c = 1



Ans. (1)

QUESTION

The combination of gates shown below yields. [AIEEE-2010]



1. XOR gate
2. NAND gate
3. OR gate
4. NOT gate

Ans. (3)

QUESTION

If a, b, c, d are inputs to a gate and x is its output, then as per the following time graph, the gate is:

[JEE Main-2016]

1. NAND
2. NOT
3. AND
4. OR

d = 0 1 0 1 0 1 0 1 0 1

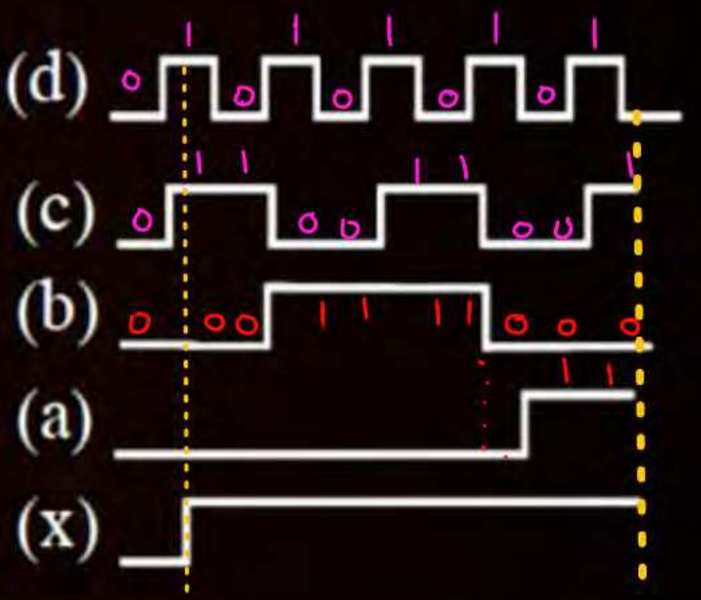
c = 0 1 1 0 0 1 1 0 0 1

b = 0 0 0 1 1 1 1 0 0 0

a = 0 0 0 0 0 0 0 0 1 1

O/P = 0 1 1 1 1 1 1 1 1 1

OR

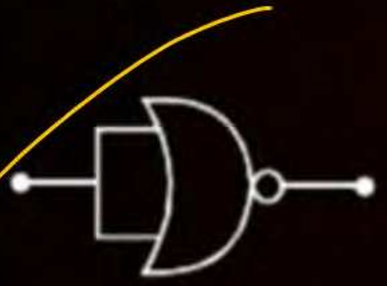
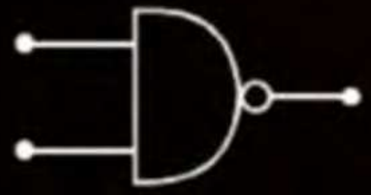


Ans. (4)

QUESTION

Which of the following gives a reversible operation?

[JEE Main-2020]

1. 
2. 
3. 
4. 

Ans : (2)

QUESTION

Identify the operation performed by the circuit given below: [JEE Main-2020]

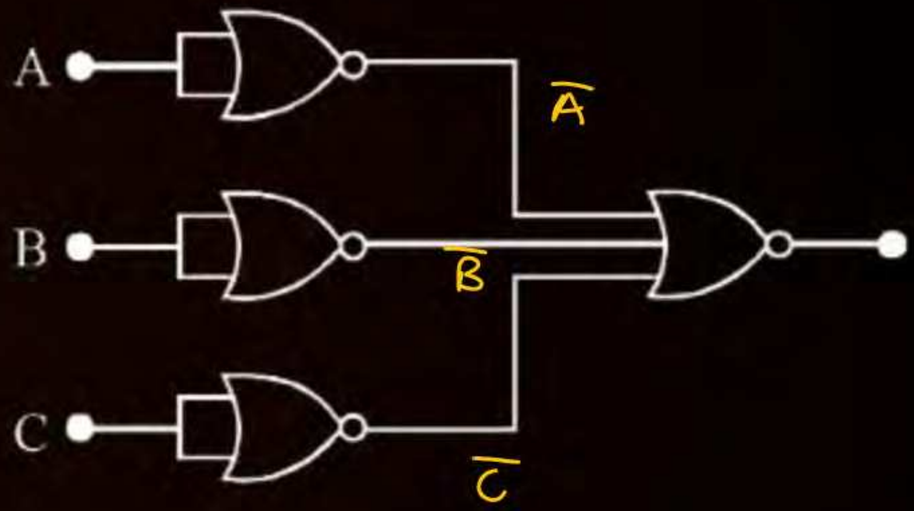
1. AND
2. NAND
3. OR
4. NOT

$$\overline{\bar{A} + (\bar{B} + \bar{C})}$$

$$= \bar{\bar{A}} \cdot \left(\overline{\bar{B} + \bar{C}}\right)$$

$$= A \cdot (\bar{\bar{B}} \cdot \bar{\bar{C}})$$

$$= A \cdot B \cdot C$$



Ans : (1)

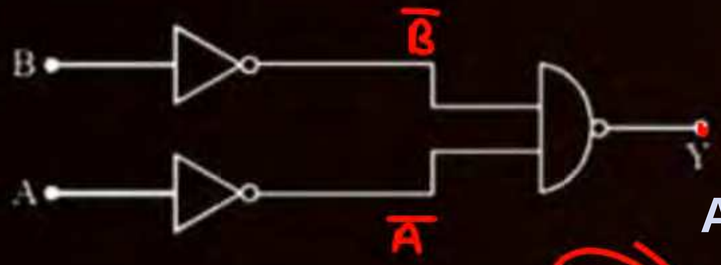
QUESTION

JISAT.

Identify the correct output signal Y in the given combination of gates (as shown) for the given inputs A and B.

[JEE Main-2020]

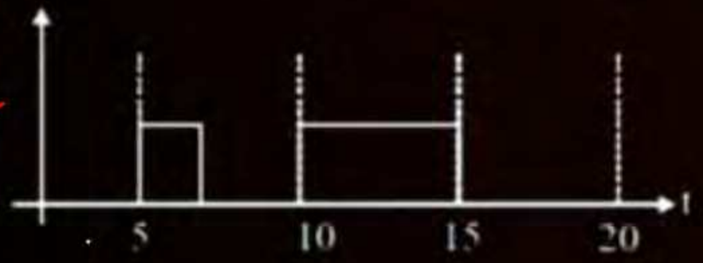
$Y = \overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$



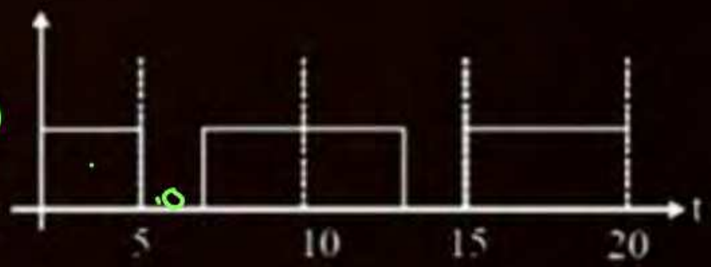
A ≡

OR

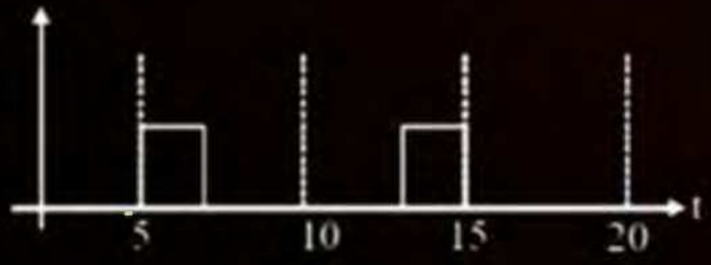
1



2



3



4

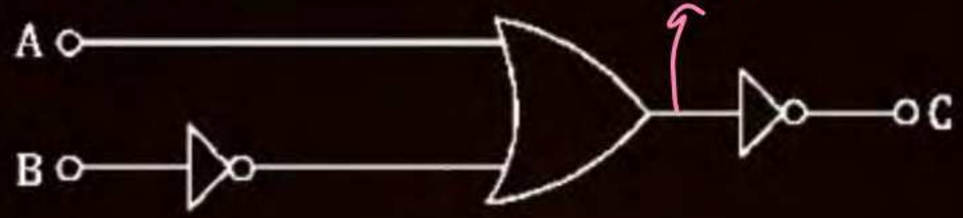
Ans : (3)

QUESTION

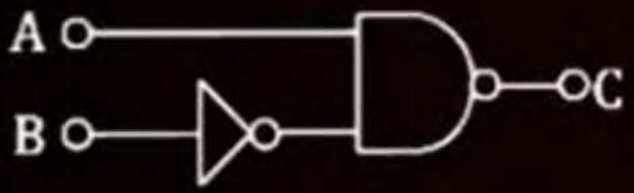
The logic circuit shown above is equivalent to : [JEE Main-2021]

$\overline{A+\overline{B}} = \overline{A}.\overline{\overline{B}}$

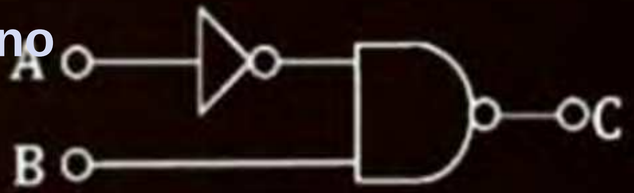
$= \overline{A}.B$



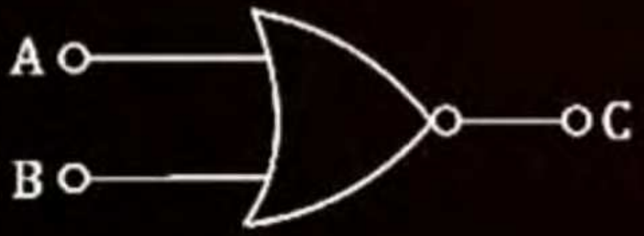
1



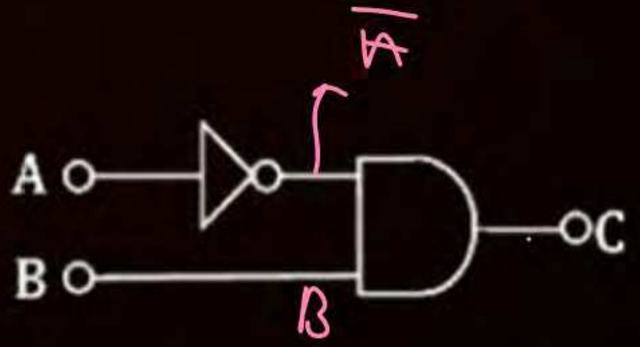
2



3



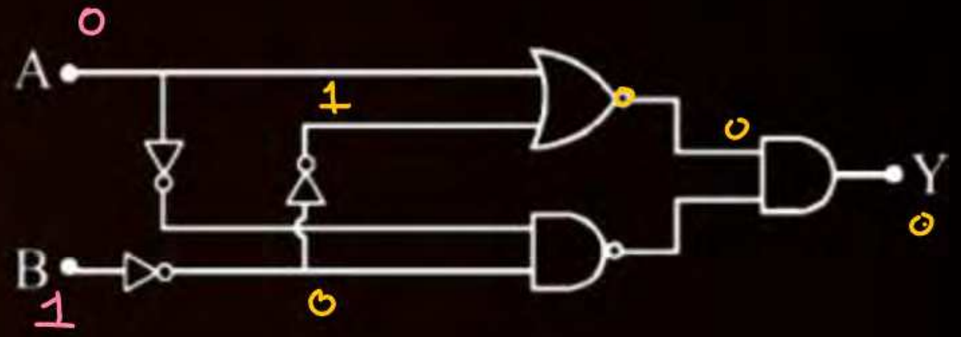
4



Ans : (4)

QUESTION

In the logic circuit shown in the figure, if input A and B are 0 to 1 respectively, the output at Y would be 'x'. The value of x is _____. **[JEE Main-2021]**

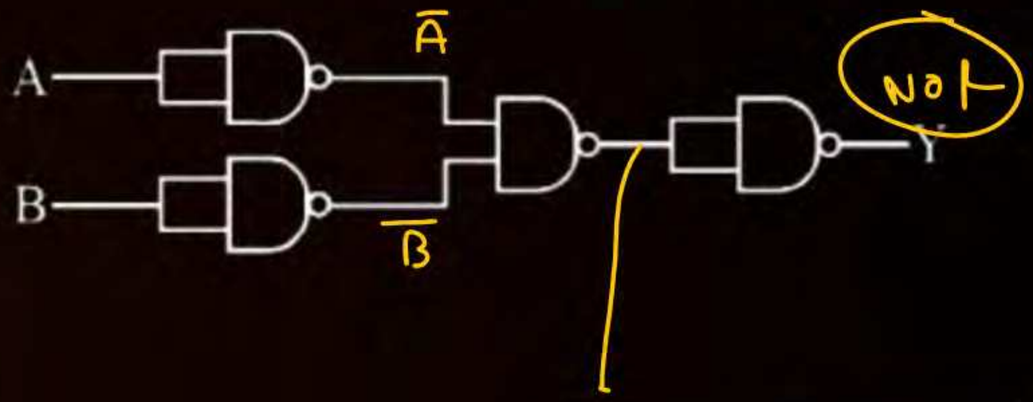


Ans : (0)

QUESTION

The following logic gate is equivalent to:

[JEE Main-2021]



1. NOR Gate
2. OR Gate
3. AND Gate
4. NAND Gate

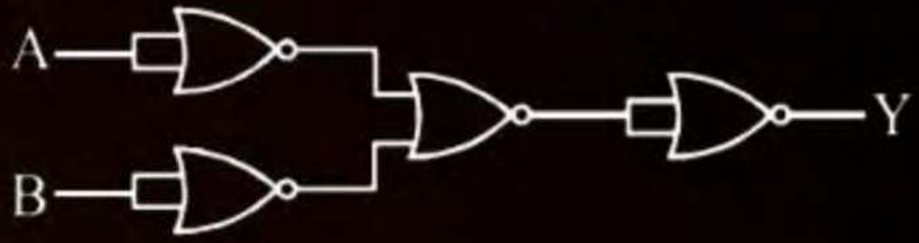
$\overline{\overline{A}.\overline{B}} = \overline{\overline{A}} + \overline{\overline{B}} = A + B$

Ans : (1)

QUESTION

The output of the given combination gates represents:

[JEE Main-2021]



1. XOR Gate
2. NAND Gate
3. AND Gate
4. NOR Gate

Ans : (2)

QUESTION

Identify the logic operation carried out by the given circuit: [JEE Main-2021]

1. OR
2. AND
3. NOR
4. NAND

$Z = \overline{A} \cdot \overline{B}$

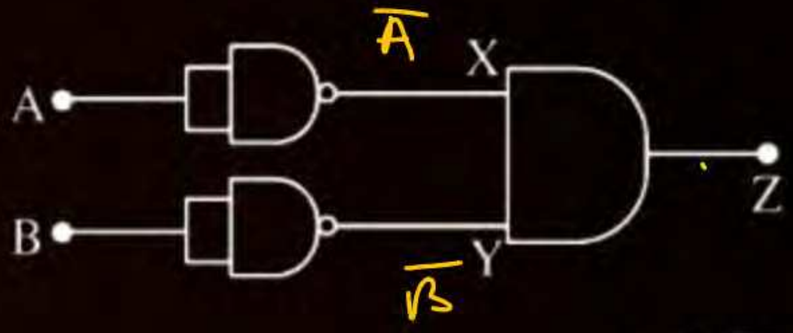
$\overline{Z} = \overline{\overline{A} \cdot \overline{B}} = \overline{\overline{A}} + \overline{\overline{B}}$

$= A + B$

$\overline{Z} = A + B$

$Z = \overline{A + B}$

NOR



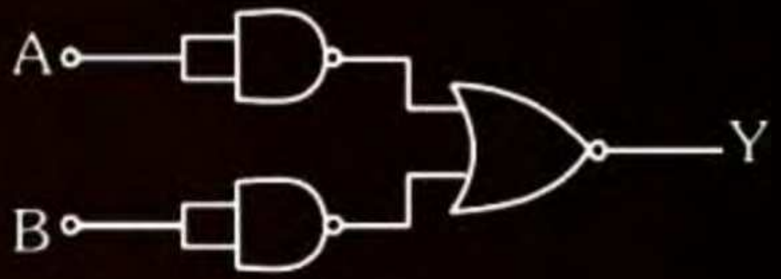
ATDB.uno

Ans : (3)

QUESTION

Identify the logic operation carried out.

[JEE Main-2021]



1. OR
2. AND
3. NOR
4. NAND

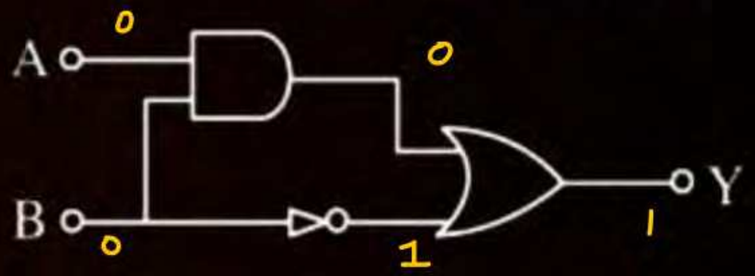
Ans : (2)

QUESTION

Find the truth table for the function Y of A and B represented in the following figure.

[JEE Main-2021]

A = 0
B = 0
} 1



1

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	0

2

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

3

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

4

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

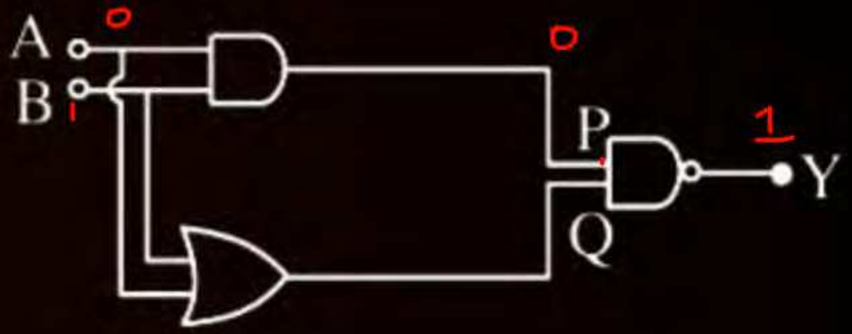
Ans : (2)

QUESTION

In the following logic circuit the sequence of the inputs A, B are (0, 0), (0, 1), (1, 0) and (1, 1). The output Y for this sequence will be:

[JEE Main-2021]

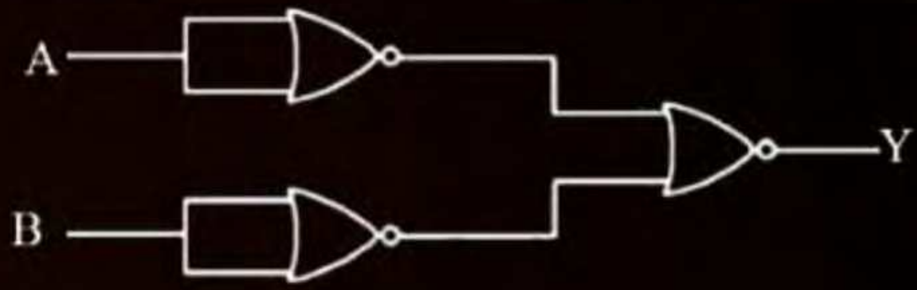
1. 1, 0, 1, 0
2. 0, 1, 0, 1
3. 1, 1, 1, 0
4. 0, 0, 1, 1



Ans : (3)

QUESTION

Identify the logic operation performed by the given circuit: **[JEE Main-2022]**



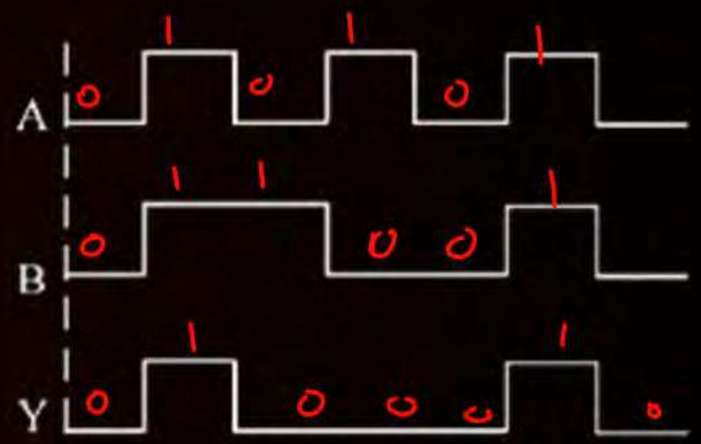
1. AND gate
2. OR gate
3. NOR gate
4. NAND gate

Ans : (1)

QUESTION

A logic gate circuit has two input A and B and Y. The voltage waveforms of A, B and Y are shown below The logic gate circuit is:

[JEE Main-2022]



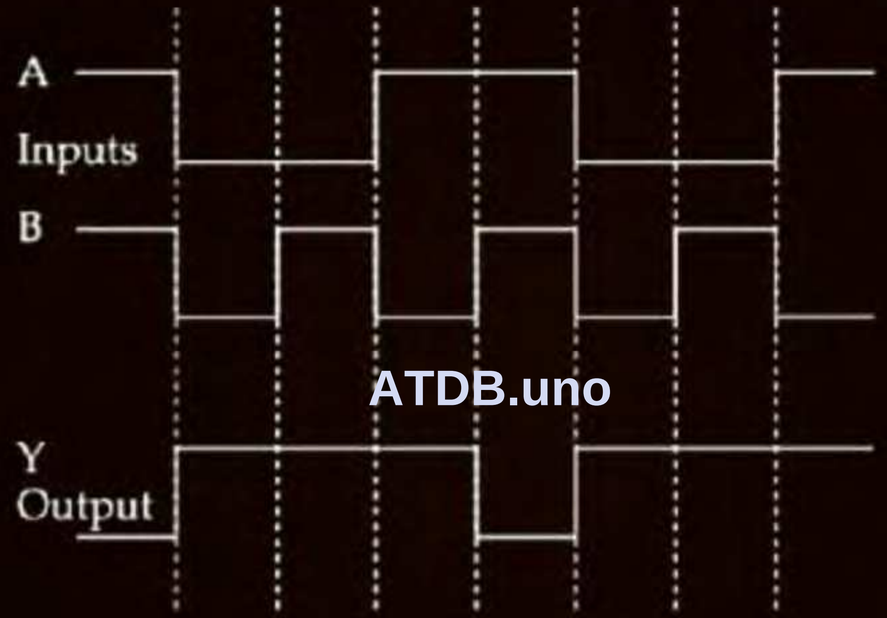
1. AND gate
2. OR gate
3. NOR gate
4. NAND gate

Ans : (1)

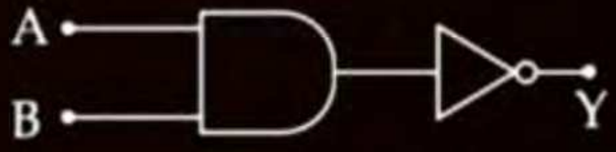
QUESTION

Identify the correct Logic Gate for the following output (Y) of two inputs A and B.

[JEE Main-2022]



1. 

2. 

3. 

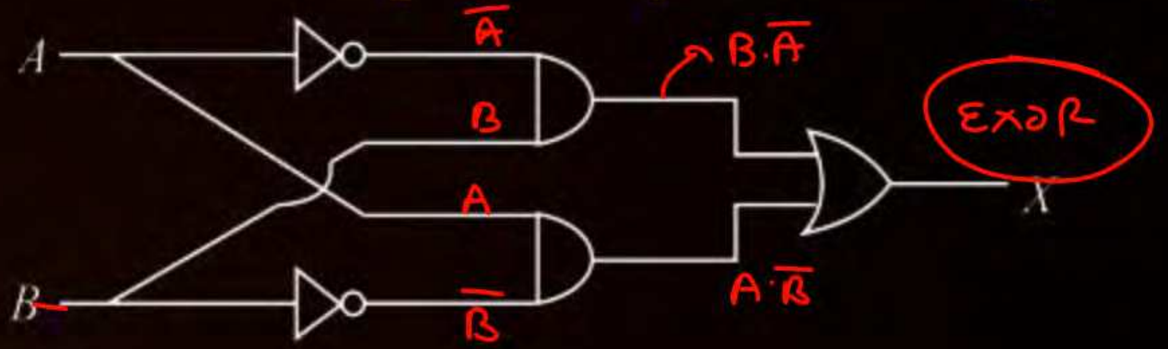
4. 

Ans : (2)

QUESTION

For the given logic gates combination, the correct truth table will be:

[29 January 2023 – Shift 2]



1

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

2

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

3

A	B	X
0	0	1
0	1	0
1	0	1
1	1	0

4

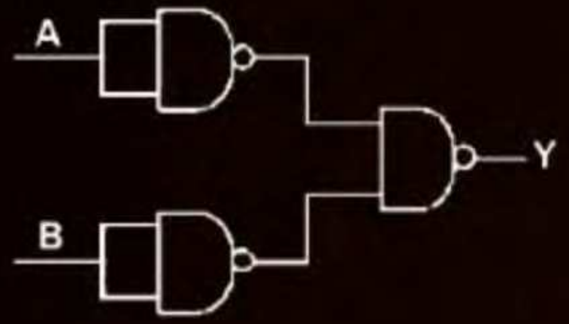
A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

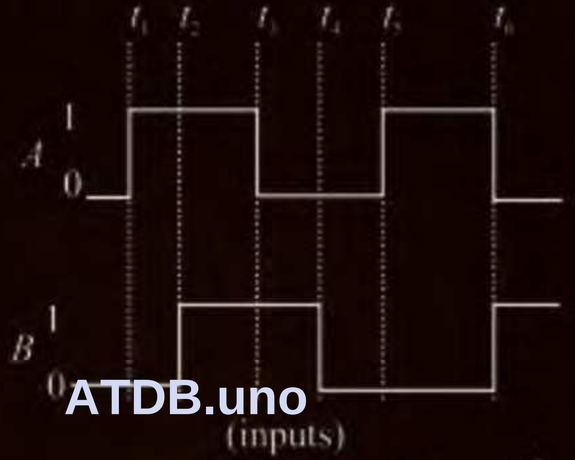
Ans : (2)

QUESTION

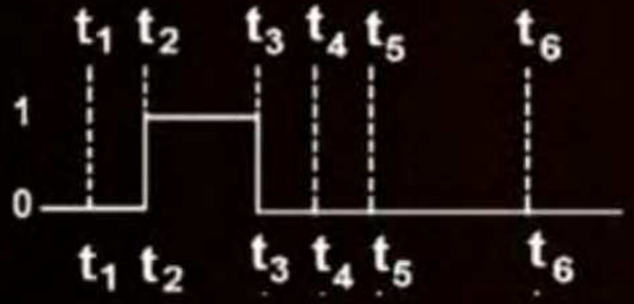
The output waveform of the given logical circuit for the following inputs A and B as shown below, is:

[30 January 2023 – Shift 1]





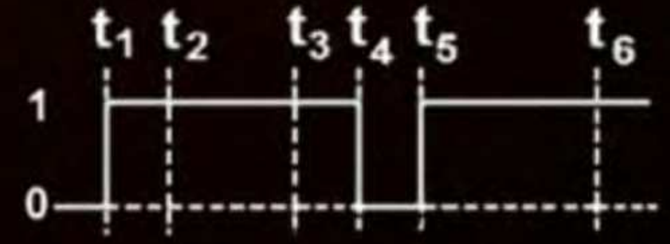
1



2

3

4

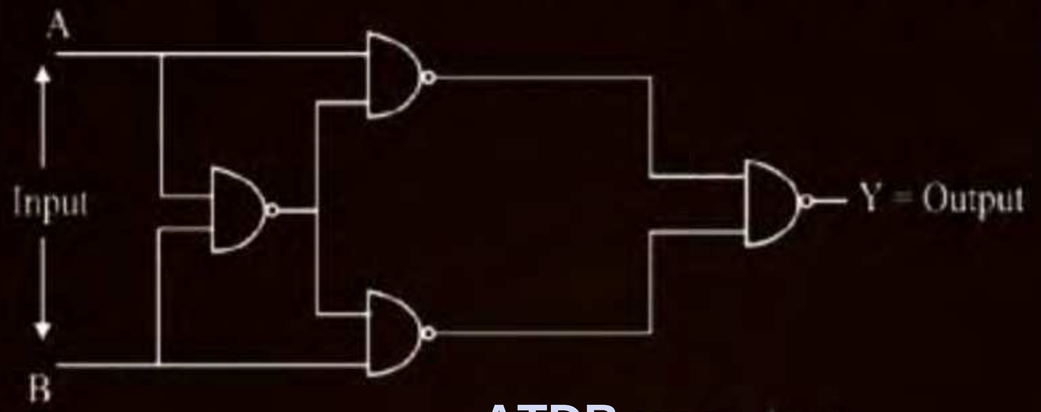


Ans : (4)

QUESTION

The output Y for the inputs A and B of circuit is given by. True table of the shown circuit is:

[30 January 2023 – Shift 2]



1

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

2

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

3

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

4

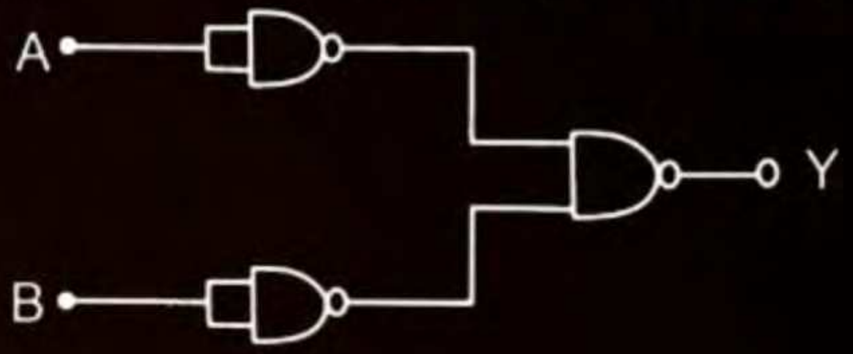
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

Ans : (4)

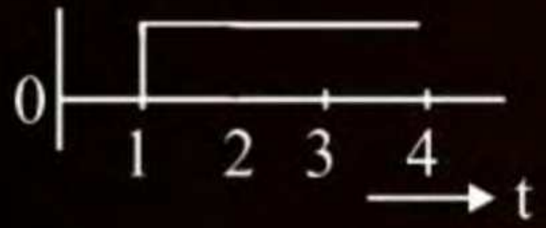
QUESTION

For the logic circuit shown, the output waveform at Y is

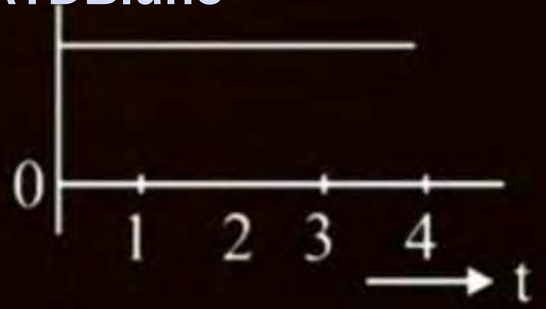
[08 April 2023 – Shift 1]



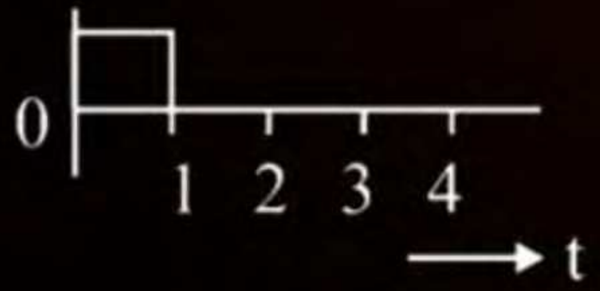
1



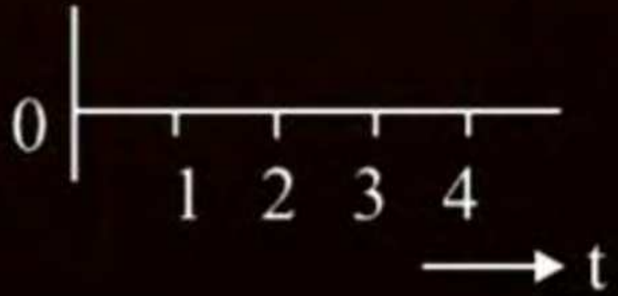
2



3



4



Ans : (1)

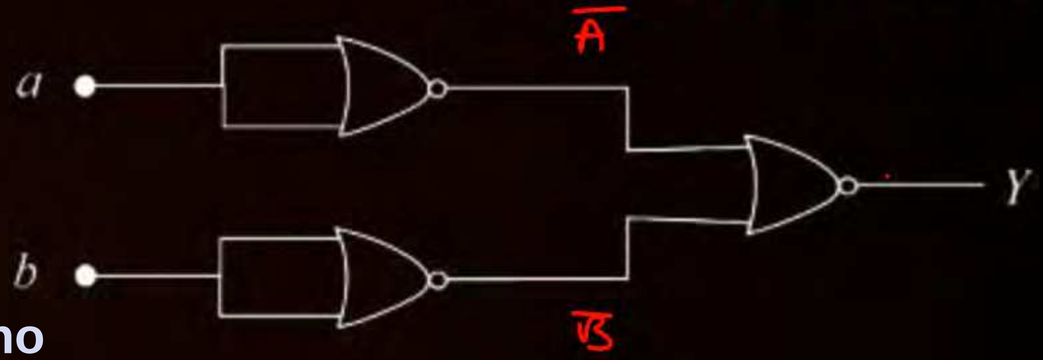
QUESTION

The logic performed by the circuit shown in figure is equivalent to:

[11 April 2023 – Shift 1]

1. AND
2. NOR
3. OR
4. NAND

$\overline{\overline{A}+\overline{B}}$



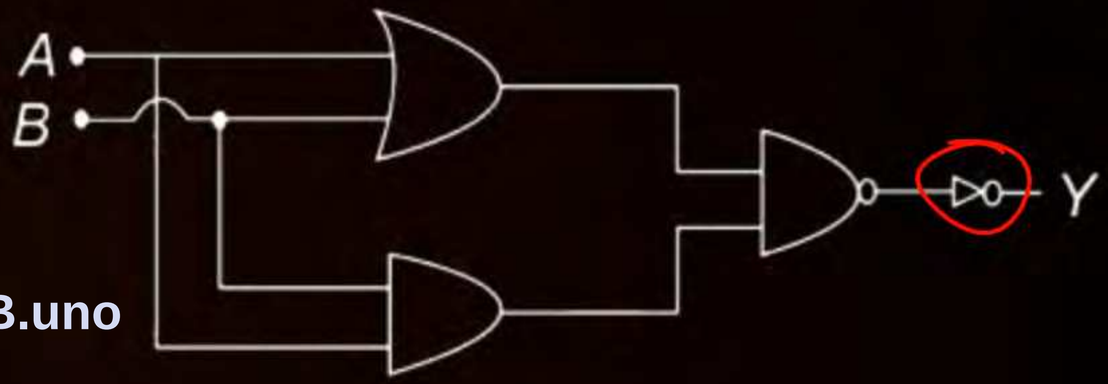
Ans : (1)

QUESTION

The logic operations performed by the given digital circuit is equivalent to:

[11 April 2023 – Shift 2]

1. NOR
2. AND
3. OR
4. NAND

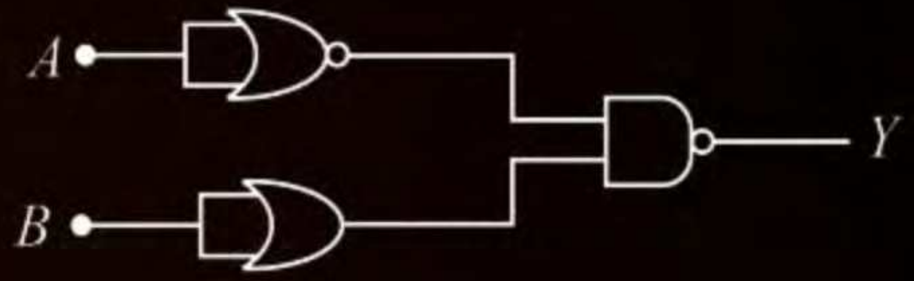


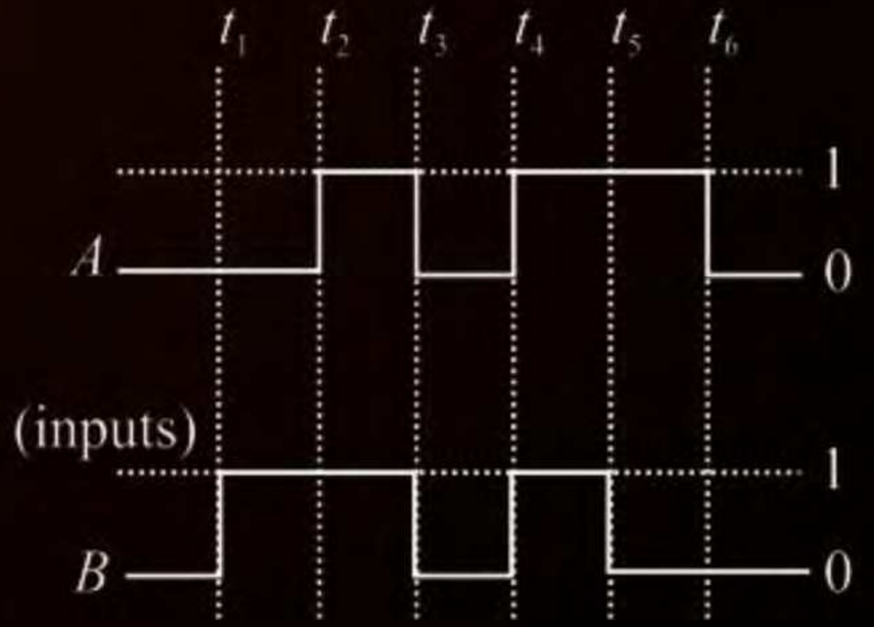
Ans : (2)

QUESTION

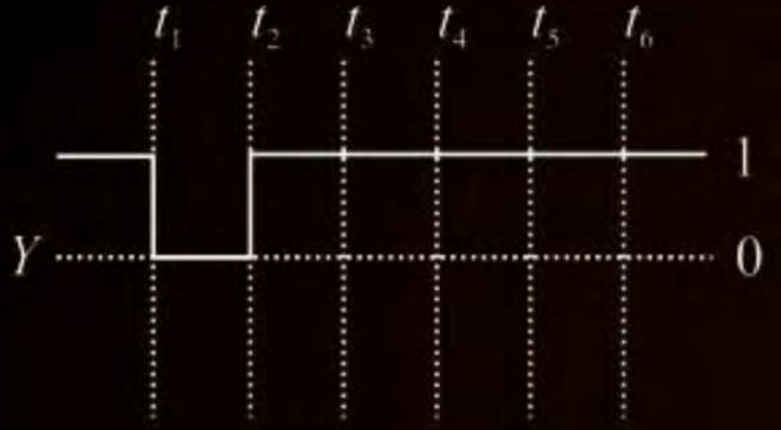
For the following circuit and given inputs A and B, choose the correct option for output 'Y'

[13 April 2023 – Shift 1]

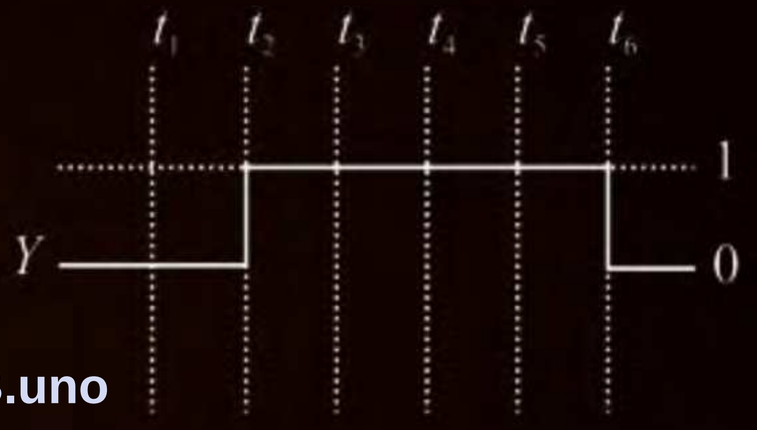




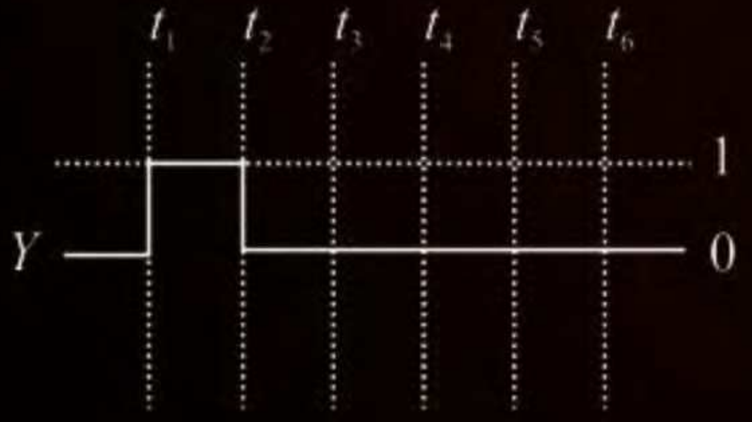
1



2



3



4

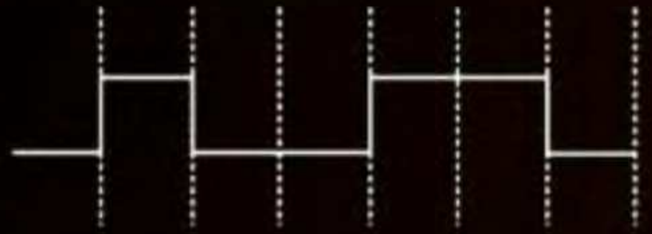
Ans : (1)

QUESTION

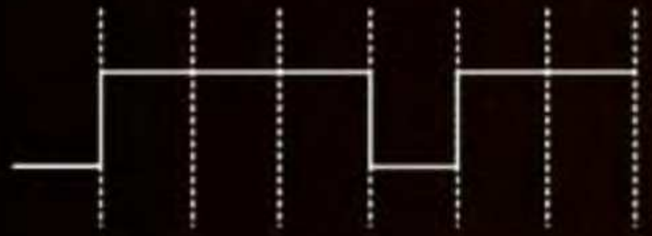
The output from a NAND gate having inputs A and B given below will be:

[13 April 2023 – Shift 2]

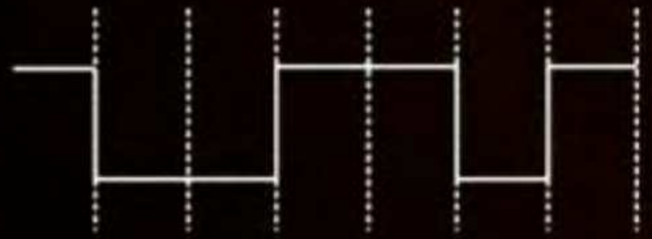
1



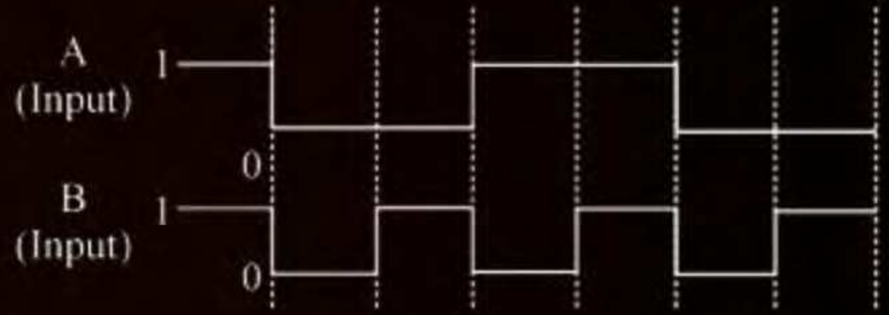
2



3



4

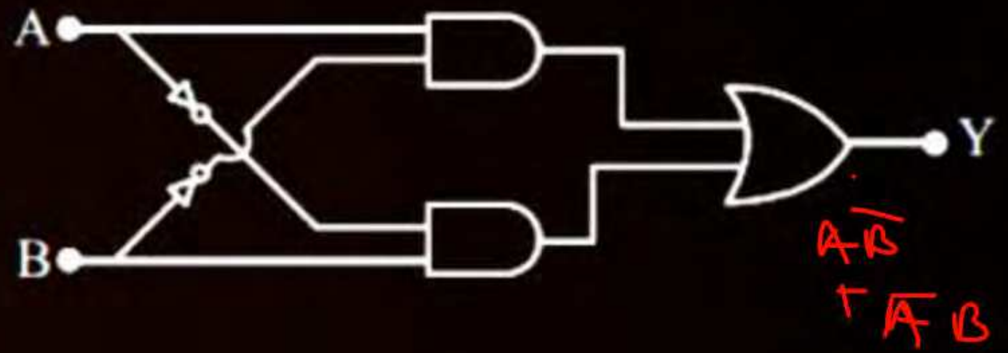


Ans : (2)

QUESTION

The truth table of the given circuit diagram is:

[27 Jan. 2024 - Shift 2]



1

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

2

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

3

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

4

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

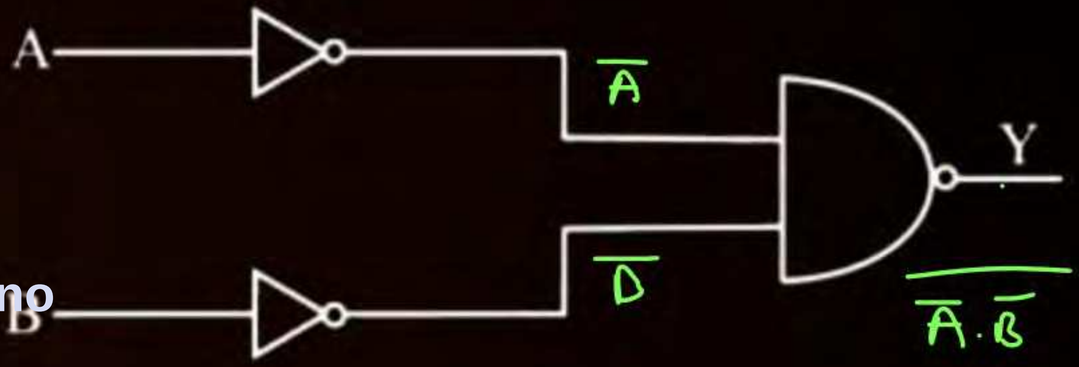
Ans : (2)

QUESTION

Identify the logic operation performed by the given circuit.

[31 Jan. 2024 - Shift 1]

1. NAND
2. NOR
3. OR
4. AND



Ans : (3)

QUESTION

The output of the given circuit diagram is:

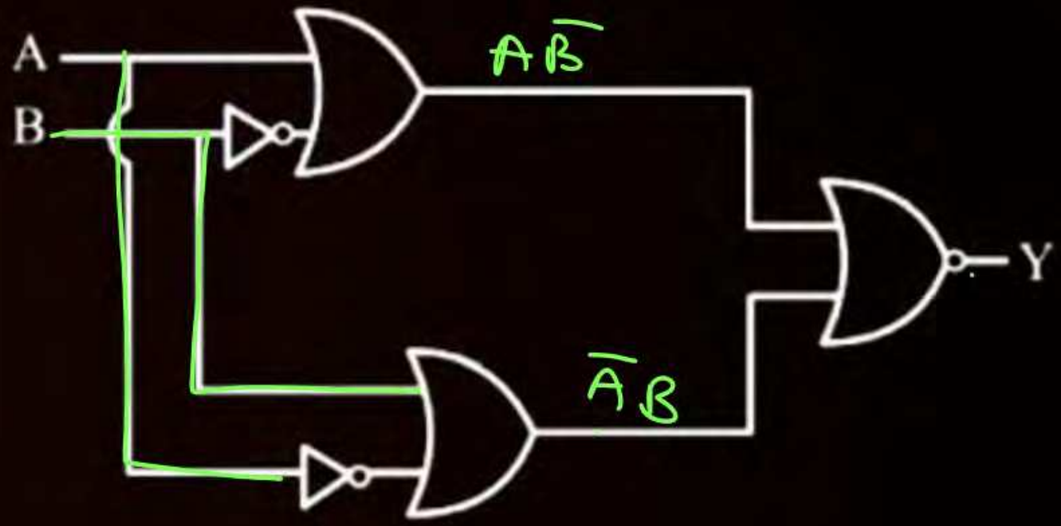
[31 Jan. 2024 - Shift 2]

1

A	B	Y
0	0	0
1	0	0
0	1	0
1	1	1

2

A	B	Y
0	0	0
1	0	1
0	1	1
1	1	0



3

A	B	Y
0	0	0
1	0	0
0	1	0
1	1	0

4

A	B	Y
0	0	0
1	0	0
0	1	1
1	1	0

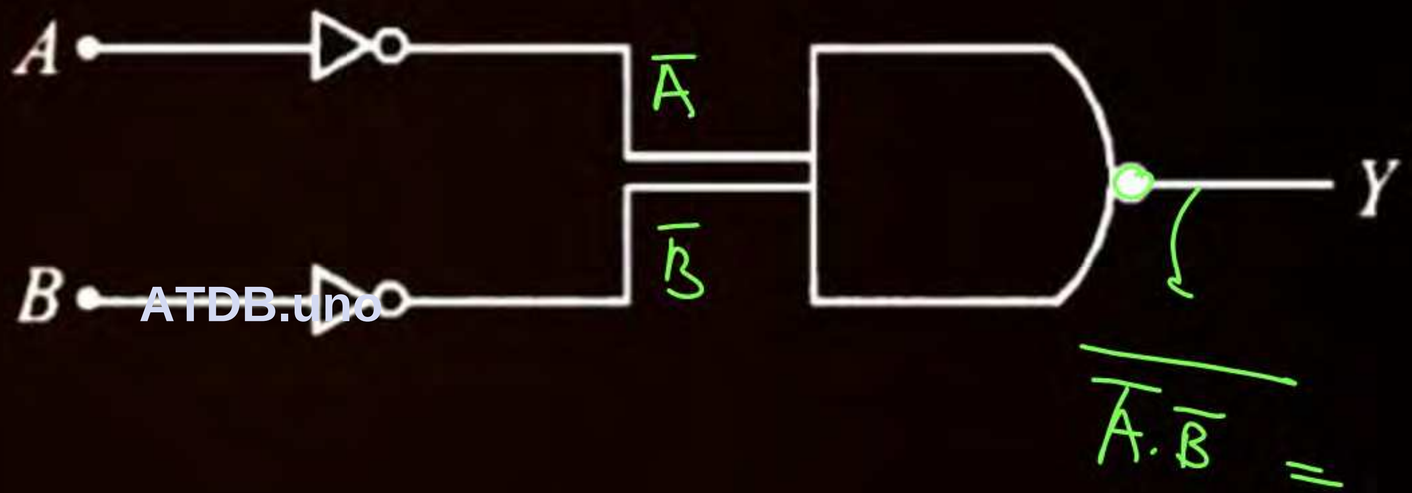
Ans : (3)

QUESTION

Identify the logic gate given in the circuit:

[04 Apr. 2024 - Shift 2]

1. NAND-gate
2. AND-gate
3. NOR-gate
4. OR-gate

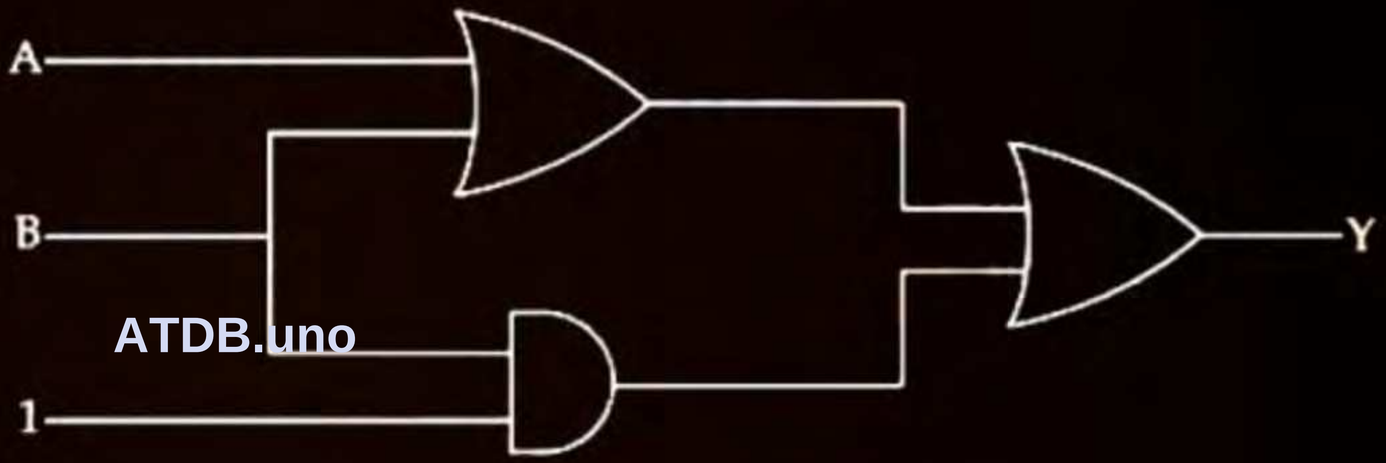


Ans : (4)

QUESTION

The output (Y) of logic circuit given below is 0 only when: [05 Apr. 2024 - Shift 2]

1. A = 1, B = 0
2. A = 0, B = 1
3. A = 0, B = 0
4. A = 1, B = 1



Ans : (3)

QUESTION

The correct truth table for the following logic circuit is:

[06 Apr. 2024 - Shift 1]

1

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	1

2

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	1

3

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

4

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Ans : (1)

QUESTION

The output Y of following circuit for given inputs is:

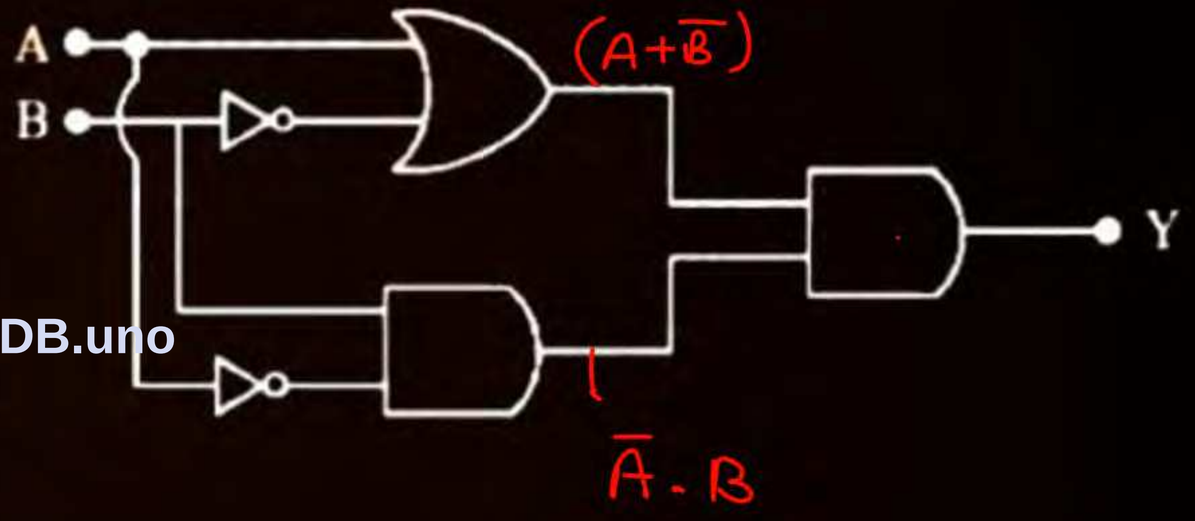
[08 Apr. 2024 - Shift 1]

1. $A \cdot B(A + B)$
2. 0
3. $\overline{A} \cdot B$
4. $A \cdot B$

$(A+\overline{B}) \cdot (\overline{A} \cdot B)$

$= A \cdot (\overline{A} \cdot B) + \overline{B} \cdot (\overline{A} \cdot B)$

$= 0 + 0$

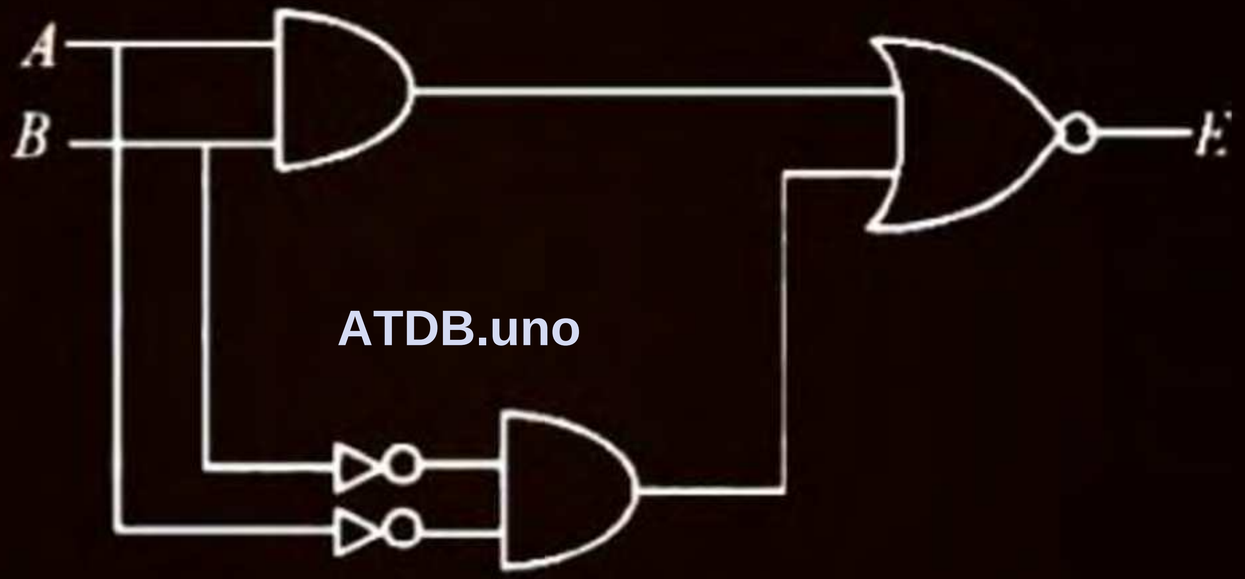


Ans : (2)

QUESTION

In the truth table of the above circuit the value of X and Y are: **[09 Apr. 2024 - Shift 2]**

1. 0, 0
2. 1, 1
3. 1, 0
4. 0, 1

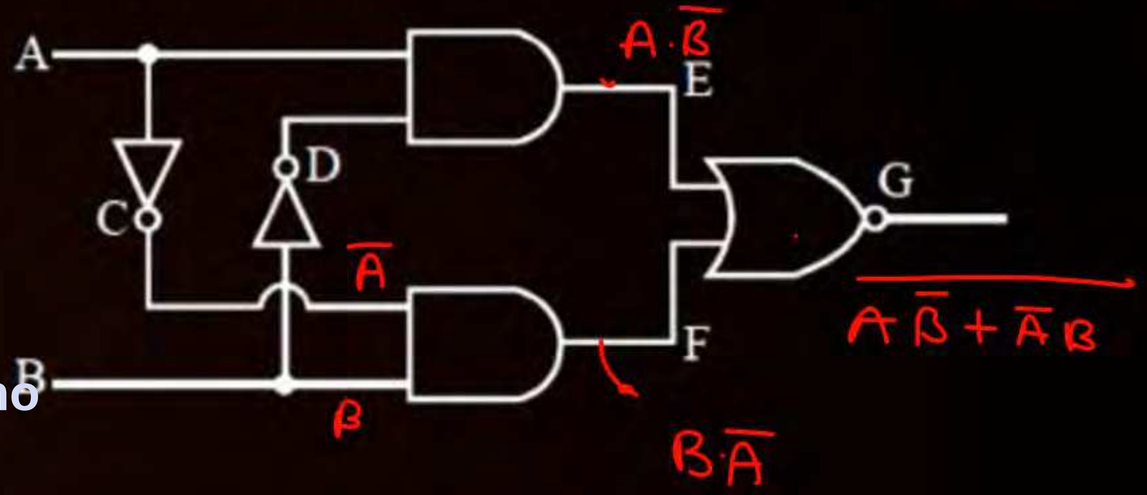


A	B	E
0	0	0
0	1	X
1	0	Y
1	1	0

Ans : (2)

QUESTION

Write a truth table for the circuit in figure, including the states at C, D, E, F and G.



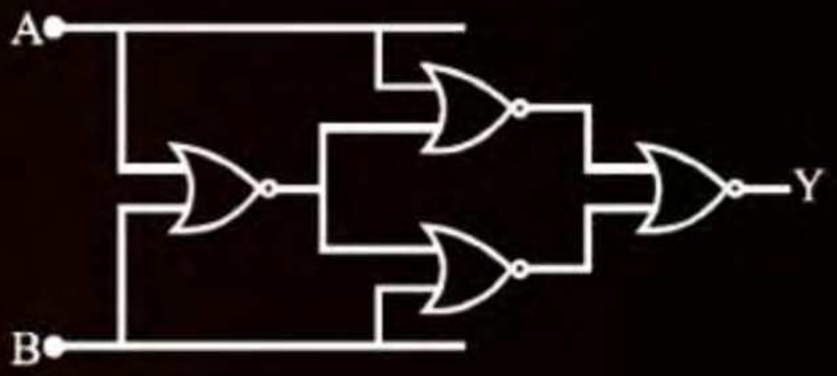
Ans.

A	B	C	D	E	F	G
0	0	1	1	0	0	1
0	1	1	0	0	1	0
1	0	0	1	1	0	0
1	1	0	0	0	0	1

QUESTION

A system of four gates is set up as shown. The 'truth table' corresponding to this system is:

[JEE-Main Online-2013]



1

A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

2

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

3

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

4

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Ans. (4)

QUESTION

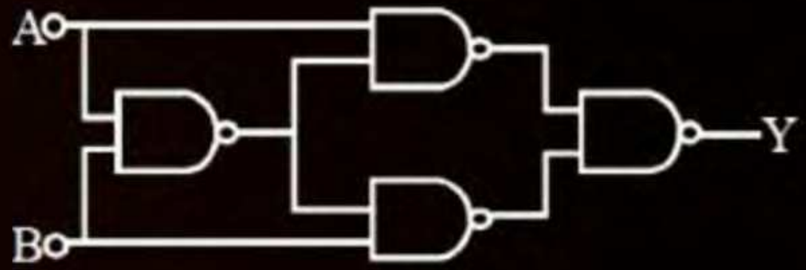
Truth table for system of four NAND gates as shown in figure is: **[AIEEE-2012]**

1

A	B	Y
0	0	1
0	1	1
1	0	0
1	1	0

2

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1



3

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

4

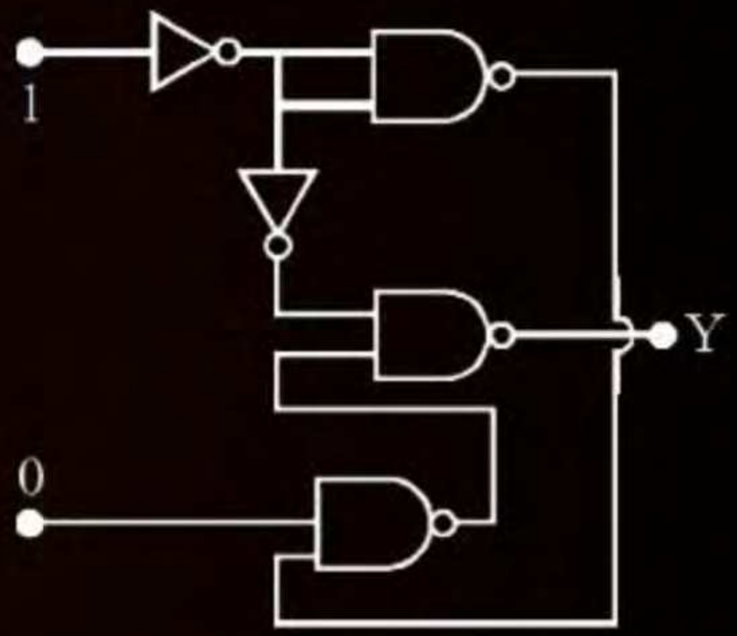
A	B	Y
0	0	0
0	1	0
1	0	1
1	1	1

Ans. (3)

QUESTION

In the given circuit, value of Y is:

[JEE Main-2020]



1. will not execute
2. 0
3. toggles between 0 and 1
4. 1

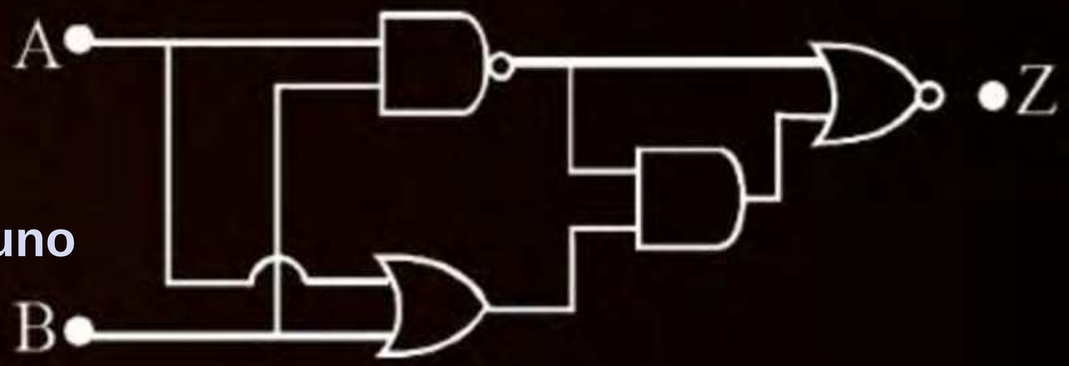
Ans : (2)

QUESTION

In the following digital circuit, what will be the output at 'Z', when the input (A, B) are (1, 0), (0, 0), (1, 1), (0, 1):

[JEE Main-2020]

1. 1, 0, 1, 1
2. 0, 1, 0, 0
3. 0, 0, 1, 0
4. 1, 1, 0, 1



Ans : (3)

QUESTION

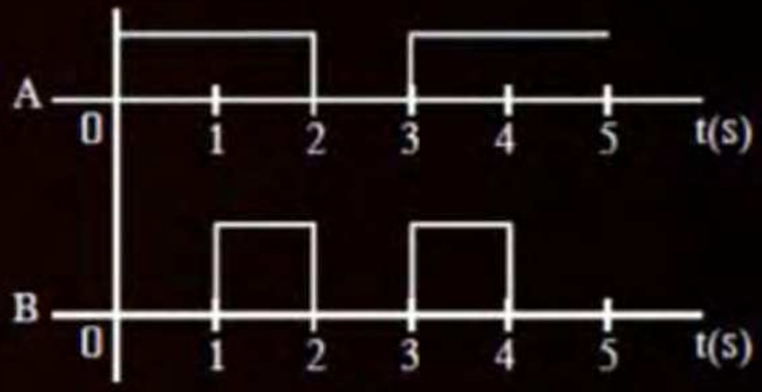
Draw the output signal Y in the given combination of gates: **[JEE Main-2021]**

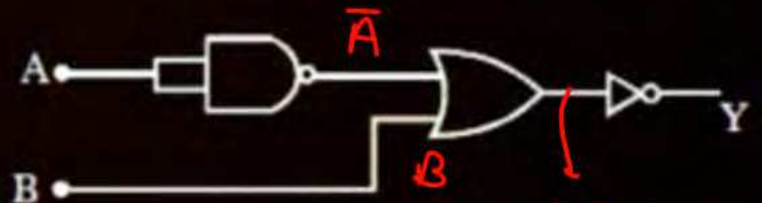
1

2

3

4



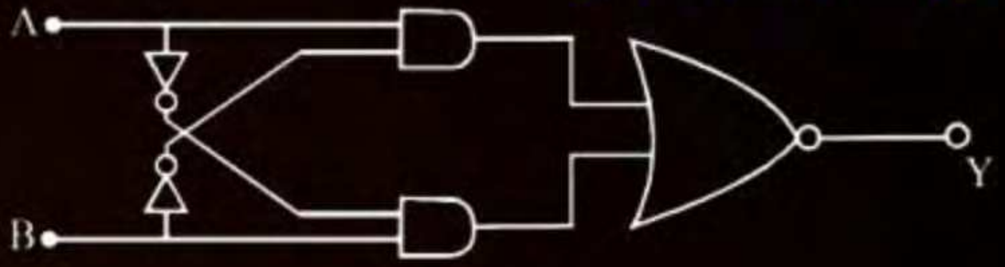


$= \overline{\bar{A} \cdot \bar{B}} = A\bar{B}$

Ans : (4)

QUESTION

The truth table for the following logic circuit is : [JEE Main-2021]



1

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

2

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

3

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

4

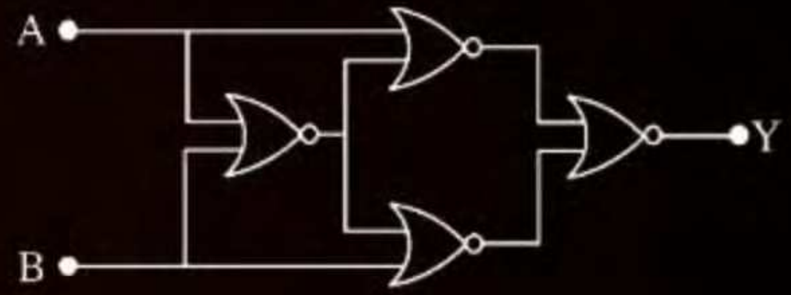
A	B	Y
0	0	0
0	1	1
1	0	0
1	1	1

Ans : (2)

QUESTION

Four NOR gates are connected as shown in figure. The truth table for the given figure is:

[JEE Main-2021]



1

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

2

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

3

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	1

4

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

Ans : (4)

QUESTION

The truth table for this given circuit is:

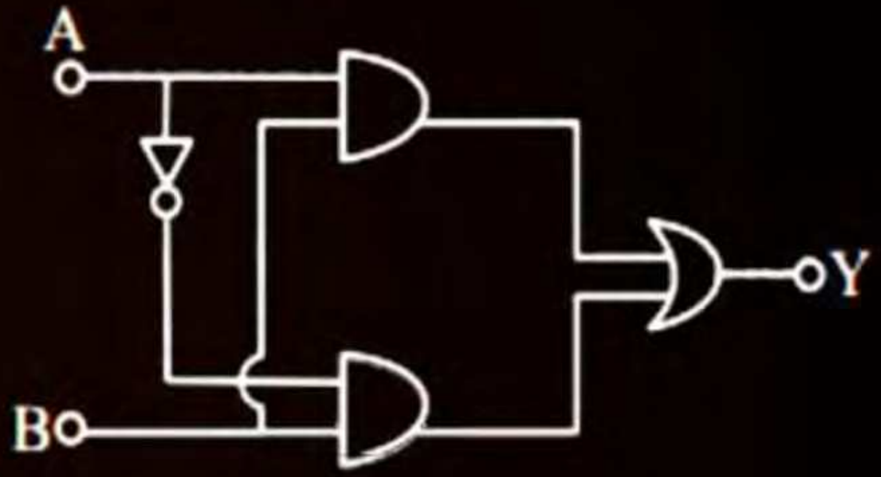
[29 Jan. 2024 - Shift 2]

1

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

2

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	1



3

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

4

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

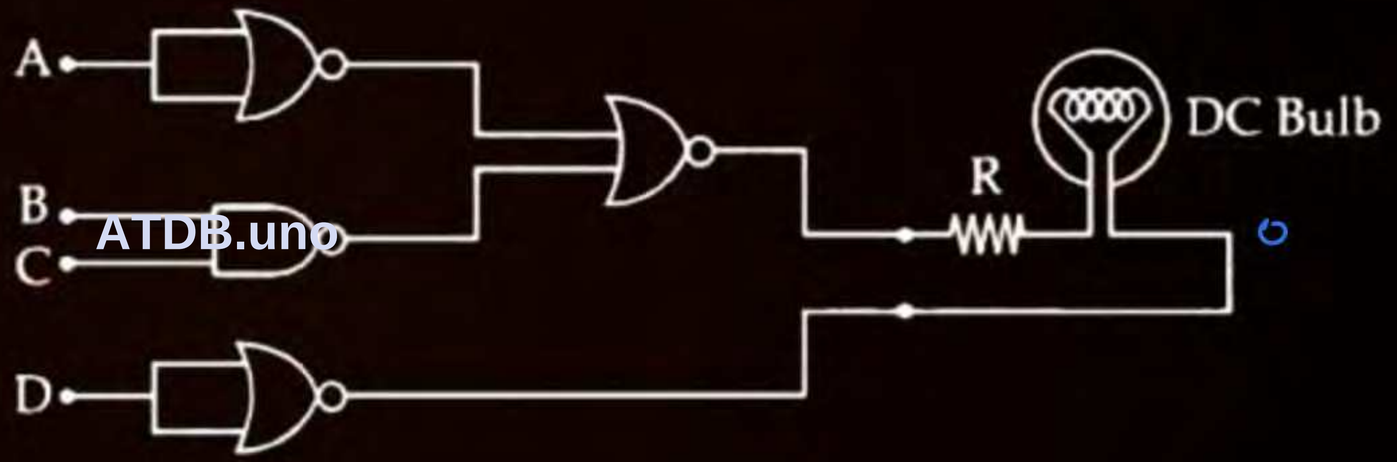
Ans : (2)

QUESTION

Following gates section is connected in a complete suitable circuit. For which of the following combination, bulb will glow (ON):

[05 Apr. 2024 - Shift 1]

1. A = 0, B = 0, C = 0, D = 1
2. A = 0, B = 1, C = 1, D = 1
3. A = 1, B = 0, C = 0, D = 0
4. A = 1, B = 1, C = 1, D = 0



Ans : (3)